OPERATING AND SERVICE MANUAL

HIGH RESOLUTION COUNTER

5307A

HEWLETT hp PACKARD

SECTION IX G

HIGH RESOLUTION COUNTER

5307A

OPERATING AND SERVICE MANUAL

SERIAL PREFIX: 1308A

This section applies directly to HP Model 5307A High Resolution Counters having serial number prefix 1308A. Insert this document into the 5300 Measuring System manual.

NEWER INSTRUMENTS

This manual with enclosed "Manual Changes" sheet(s) applies directly to HP Model 5307A High Resolution Counters having serial number prefixes listed on the "Manual Changes" sheets.

Printed: JUN 1975

MANUAL PART NO. 05307-90004
MICROFICHE PART NO. 05307-90005

PRINTED IN U.S.A.

HEWLETT hp PACKARD

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SUBSECTION I
GENERAL INFORMATION

9G-1-1. INTRODUCTION

9G-1-2. This subsection of the manual explains the purpose and use of Section IX G of the HP 5300 Measuring System documentation, gives a description of the HP 5307A High Resolution Counter (see Figure 9G-1-1), and provides instrument identification and specifications information.

9G-1-3. PURPOSE AND USE OF SECTION IX G

9G-1-4. Section IX G contains the information necessary to install, operate, and maintain the high resolution counter. Parts lists, component-locator illustrations, and a schematic diagram are included. Insert this document in the HP 5300 Measuring System manual as part of Section IX.

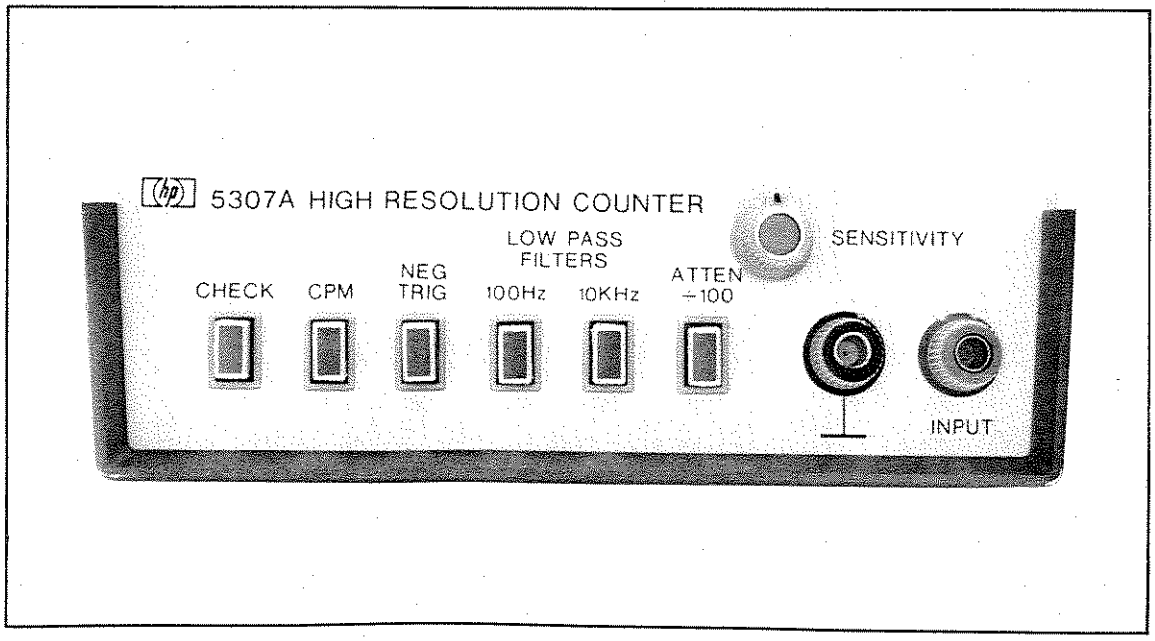
9G-1-5. INSTRUMENT DESCRIPTION

9G-1-6. When plugged onto a 5300 mainframe, the high resolution counter can measure frequencies between 5 Hz and 2 MHz or 50 CPM (counts per minute) and 10,000,000 CPM. The measured frequency is displayed with six digits of resolution. Front-panel switches select positive or negative triggering, input attenuation, and low-pass filtering. All electrical and mechanical specifications are listed in Table 9G-1-1.

9G-1-7. INSTRUMENT IDENTIFICATION

9G-1-8. Hewlett-Packard uses a two-section, nine-digit serial number (0000A00000) mounted on the rear panel to identify the instrument. The first four digits are the serial prefix and the last five digits refer to the specific instrument. If the serial prefix on your instrument differs from

Figure 9G-1-1. Model 5307A High Resolution Counter



that listed on the title page of this section, there are differences between the manual and your instrument. Lower serial prefixes are documented in Subsection VII and higher serial prefixes are covered by a manual change sheet included with the manual.

9G-1-9. The printed circuit board within the instrument is identified by a two-section, 10-digit part number (e.g., 05307-60001) and a four-digit series number (e.g., "SERIES 1140A"). The series number identifies the electrical characteristics of the complete printed-circuit assembly. A replacement circuit-board assembly may have a different series number than the assembly originally supplied with the instrument. Therefore, when troubleshooting a circuit-board assembly, ensure that the series number on the schematic diagram matches the series number on the board assembly. If the series number on the assembly is lower than the number on the schematic diagram in Subsection VIII, refer to Subsection VII of this document for change information. If the series number on the assembly is higher than the number on the schematic diagram in Subsection VIII, the change information is provided in a manual change sheet which is available from the nearest Hewlett-Packard Sales and Service Office.

Table 9G-1-1. Specifications

INPUT

Range: Hz mode 5 Hz to 2 MHz
CPM mode 50 to 10M counts/minute (0.833 Hz to 166 KHz)

Sensitivity (min):

Sinewaves	Hz	CPM
10 mV rms	5 Hz - 1.2 MHz	120 CPM - 10M CPM
25 mV rms	1.2 MHz - 2.0 MHz	50 CPM - 120 CPM

Pulses

For low duty cycle pulses (<15%)

15 mV peak for 250 nsec pulses

100 mV peak for 100 nsec pulses

Basic sensitivity can be varied continuously up to 2.5 V rms by adjusting sensitivity control.

Attenuator: ÷1 or ÷100 effectively raises basic input sensitivity by a factor of 100 (10 mV→2.5 V to 1 V→250 V)

Low Pass Filters (3 dB Point):	100 Hz	10 KHz
Max Attenuation	60 dB	40 dB
Roll off	20 dB per decade	20 dB per decade

Impedance: No filters, 1 MΩ shunted by <50 pF
100 Hz filter, 1 MΩ shunted by series combination of 100 KΩ and .015 μF
10 KHz filter, 1 MΩ shunted by series combination of 100 KΩ and 150 pF

Coupling: ac

Overload Protection: 200 V rms below 10 kHz
2×10^6 V Hz (voltage times frequency) rms to 0.4 MHz
5 V rms above 0.4 MHz,
with ÷100 attenuator, 300V rms

Trigger Level: Selectable positive or negative for optimum triggering from sinusoidal inputs or pulses

Table 9G-1-1. Specifications (Continued)

FREQUENCY MEASUREMENT

Periods Averaged: Automatically selected for maximum resolution. Two periods are averaged for signals up to 100 Hz. For each decade increase in the input signal the number of periods averaged increases by a factor of 10 up to 200,000 periods averaged above 1 MHz.

Measurement Time: Varies from 312 msec for a display of 170000 to 815 msec for a display of 999000.
Hold-off adjustable from .35 μsec to 3.5 μsec and 1 msec to 10 msec.

Accuracy: $\pm 3 \times 10^{-5}$* ± 1 count ± trigger error** ± time base error.

*$\pm 3 \times 10^{-5}$ is due to reciprocating scheme and is worst case.
**Trigger error is less than ±.03% of one period ÷ periods averaged for sine waves with 40 dB or better signal to noise ratio.

Display: In Hz mode; Hz and MHz with automatically positioned decimal point.
In CPM mode; M with automatically positioned decimal point.

GENERAL

Check: Measures internal reference frequency. Displays 1.00000 MHz in Hz mode, 100000 M in CPM mode.

Operating Temperature: 0° to 50°C

Power Requirements: Including 5300 Mainframe, nominally 10 watts

Weight: Net 2 lbs. (0.9kg). Shipping 3¼ lbs. (1.5kg)

Dimensions (with 5300 Mainframe): Height: 3½ in. (89mm); Width: 5¼ in. (160mm); Depth: 9¾ in. (248mm).

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5307A HIGH-RESOLUTION COUNTER

SUBSECTION II
INSTALLATION

9G-2-1. UNPACKING AND INSPECTION

9G-2-2. If the shipping carton is damaged, ask that the carrier's agent be present when the instrument is unpacked. Inspect the instrument for damage such as scratches, dents, broken knobs, etc. If the instrument is damaged or fails to meet performance tests when used with the 5300 mainframe, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. Performance check procedures are located in Subsection V, and Sales and Service Offices are listed in Section VI of the 5300 portion of the manual. Retain the shipping carton and the padding material for the carrier's inspection. The Sales and Service Office will arrange for the repair or replacement of the instrument without waiting for the claim against the carrier to be settled.

9G-2-3. STORAGE AND SHIPMENT

9G-2-4. PACKAGING. To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Your Hewlett-Packard Sales and Service Office can provide packaging material such as that used for original factory packaging. Contract packaging companies in many cities can provide dependable custom packaging on short notice. The unit was originally packaged as follows:

The original container is a corrugated cardboard box with 200 lbs. burst test (HP 9211-1620). The instrument is secured and protected in the box by a top and bottom molded frame of polystyrene foam (HP No. 9220-1545).

9G-2-5. ENVIRONMENT. Conditions during storage and shipment should normally be limited as follows:

a. Maximum altitude: 25,000 ft.
b. Minimum temperature: -40°F (-40°C)
c. Maximum temperature: +167°F (+75°C)

9G-2-6. INSTALLATION AND REMOVAL OF PLUG-ON

9G-2-7. The counter must be used with a 5300 mainframe to make measurements. Mate the counter and the mainframe according to the instructions given in Section II in the 5300 mainframe documentation.

9G-2-8. PORTABLE OPERATION

9G-2-9. Use of the HP Model 5310A Battery Pack enables the 5300 mainframe and the counter to be used in areas removed from ac power sources. The battery pack provides a minimum of 3 hours operation (typically 5 hours) at 20° to 30°C operating and charging temperature. Tables 1-2 and 1-4 of the 5300 portion of the manual lists the battery pack as an available accessory. Documentation for the battery pack is also included in Section IV through VIII of the 5300 portion of the manual. To prepare the 5300/5307 for portable operation, refer to Paragraph 2-15 and Figure 2-2, of the 5300 portion of the manual.

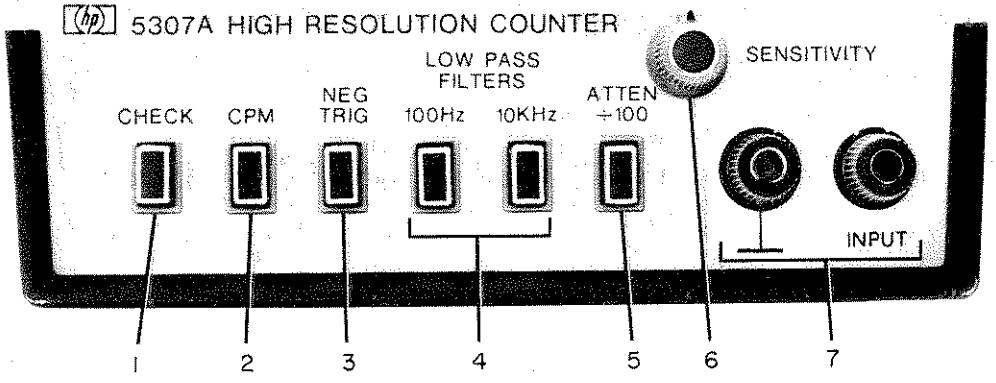
SECTION IX G
5307A HIGH RESOLUTION COUNTER

SUBSECTION III
OPERATION

9G-3-1. INTRODUCTION

9G-3-2. This subsection of the manual provides operating instructions for the counter. Descriptions of the front-panel controls and connectors are given in Figure 9G-3-1.

Figure 9G-3-1. Front-Panel Controls and Connectors



1. CHECK pushbutton. When depressed, places counter in the check mode of operation.

2. CPM pushbutton. Selects either a display in counts per minute (depressed position) or a display in Hertz (non-depressed position).

3. NEG TRIG pushbutton. Selects a negative trigger level and slope when depressed. Selects a positive trigger level and slope when in the non-depressed position.

4. LOW PASS FILTERS. The 100 Hz and 10 KHz pushbuttons, when depressed, select low pass filters with cutoff frequencies as specified.

5. ATTEN ÷ 100 pushbutton. When depressed, attenuates the input signal by a factor of 100.

6. SENSITIVITY control. Sets the sensitivity of the counter. Clockwise rotation increases sensitivity.

7. INPUT and common terminals. Used for connection of signal to be measured. Be sure to observe polarity considerations. Connect source common to counter common and the signal line to be measured to the INPUT terminal.

9G-3-3. OPERATING CONSIDERATIONS

9G-3-4. The following paragraphs describe the uses of the counter's front-panel controls with emphasis on specific measurement problems and applications.

9G-3-5. CHECK MODE. Pressing the front-panel CHECK pushbutton places the counter in the check mode of operation. Use this mode to make a quick check of overall instrument operation. Proper operation of most circuits within the counter is verified by a display of 1.00000 MHz (100 000 M if CPM pushbutton is depressed) when the counter is operated in the check mode.

9G-3-6. NORMAL OPERATING MODES. The CPM (counts per minute) pushbutton is used to select the counter's mode of operation. When the CPM pushbutton is depressed, the 5300 mainframe displays the number of pulses per minute that occur at the INPUT terminal . When the CPM switch is not depressed, the mainframe displays the input frequency in Hertz (cycles per second).

9G-3-7. TRIGGER AND SENSITIVITY SELECTION. The front-panel NEG TRIG (negative trigger) pushbutton selects a negative trigger level and slope when depressed and a positive trigger level and slope when in the non-depressed position. The SENSITIVITY control sets the signal level that is required to trigger the counter. If negative-going pulses are to be measured, depress the NEG TRIG pushbutton; if positive pulses are to be measured, leave the NEG TRIG pushbutton in the non-depressed position. Sine wave inputs can be measured with either positive or negative triggering. In all cases, adjust the sensitivity control for a stable mainframe display.

9G-3-8. SIGNAL ATTENUATION. The front-panel ATTEN ÷ 100 pushbutton is used to extend the range of possible voltage levels that may be applied to the INPUT terminal. When the ATTEN ÷ 100 pushbutton is depressed, the counter can measure signals with voltages up to 300 Vrms. When the pushbutton is in the non-depressed position, the voltage limit varies from 200 Vrms (maximum) below 10 kHz to 5 Vrms (maximum) above 400 kHz. Refer to the specifications in Table 9G-1-1 for further information. When the position of the ATTEN ÷ 100 pushbutton is changed, the SENSITIVITY control usually requires readjustment for a stable mainframe display.

9G-3-9. LOW-PASS FILTER SELECTION. Two LOW PASS FILTERS can be selected with front-panel pushbutton switches: a 100 Hz filter and a 10 kHz filter. Depressing one of the filter pushbuttons inserts the filter in the signal line; releasing the pushbutton removes the filter from the signal line. These filters provide a means for eliminating interfering signals that have frequencies above the panel-listed frequency. For example, by depressing the 10 kHz pushbutton, a 5 kHz signal will be measured by the counter while an interfering signal at 20 kHz is sharply attenuated.

9G-3-10. COUNT HOLDOFF CAPABILITY. Provision is made within the counter to adjust the length of time that the counter circuits are inhibited after counting a pulse. This feature is useful for measuring ringing signals (such as those encountered when a magnetic pickup transducer is used to generate the counter's input signal) when it is desirable to count only each pulse group and to eliminate any accumulation of counts from subsequent ringing within each pulse group. With proper adjustment, the counter will count the leading pulse of a ringing waveform and inhibit any further count accumulation until after the ringing has subsided. The counter is adjusted at the factory so the holdoff feature does not limit counting at the maximum specified frequency (see Table 9G-1-1, Specifications). For information on changing the count holdoff time, refer to the Pulse Width Adjustment procedure in Subsection V.

9G-3-11. OPERATING PROCEDURE

9G-3-12. Operate the counter according to the following procedure.

WARNING

TO AVOID POSSIBILITY OF BODILY INJURY AND/OR EQUIPMENT DAMAGE WHILE PERFORMING THE FOLLOWING PROCEDURE, BE SURE TO OBSERVE POLARITY REQUIREMENTS WHEN CONNECTING TEST LEADS. ADDITIONALLY, DO NOT EXCEED THE INPUT VOLTAGE LIMITATIONS AS SPECIFIED IN TABLE 9G-1-1.

a. Mate the counter with the 5300 mainframe as described in Subsection II, Installation.

b. Set front-panel ATTEN ÷ 100 pushbutton switch as necessary for the anticipated voltage level of the input signal. If voltage is unknown, attempt to make the measurement with the ATTEN ÷ 100 pushbutton depressed. If the counter will not provide a stable display at any setting of the SENSITIVITY control and the voltage is known to be less than the maximum limits specified in Table 9G-1-1, release the ATTEN ÷ 100 pushbutton.

c. If a display in counts per minute is desired, depress the CPM pushbutton. If a display in Hertz is desired, the CPM pushbutton must be in the non-depressed position.

d. Depress the NEG TRIG pushbutton if negative pulses are to be counted. Leave the NEG TRIG pushbutton in the non-depressed position if positive pulses are to be counted. The frequency of symmetrical waveforms can be measured with the NEG TRIG pushbutton in either position.

e. Connect suitable test leads between the counter and the signal source.

f. Turn the SENSITIVITY control fully ccw, then advance the control in the cw direction until a stable display is obtained.

SECTION IX G
5307A HIGH RESOLUTION COUNTER

SUBSECTION IV
THEORY OF OPERATION

9G-4-1. GENERAL THEORY

9G-4-2. The 5307A is a frequency counter that measures low frequencies and yields high resolution in a minimum of time, e.g., 60.0000 Hz in ½ sec. To do this, the counter makes a period average measurement of the input signal, generates an internal frequency that is proportional to the period average measurement, makes a period average measurement of the generated frequency, and displays the result as frequency. The instrument is a true reciprocal-taking counter.

9G-4-3. The following sequence of events occurs on the A1 Logic Board Assembly during each measurement cycle. First, a period average measurement of the input signal is made; that is, the Period/Frequency Generator Counter accumulates divided clock pulses, while the input signal accumulates counts in the mainframe's Time Base Counter. At the end of the measurement, the actual number of periods is recorded in an exponent counter, while the Period/Frequency Generator (P/FG) Counter contains the number of clock pulses in BCD form. Since each clock pulse represents a specific amount of time, the total amount of clock pulses represents the time it took to accumulate 10^n periods of the input signal. This clock data is multiplexed by the Counter Multiplexer, one digit at a time, and is stored in a RAM (random access memory). While these counts are being stored, the mainframe counter that totalized the input signal is being reset: The exponent counter retains a BCD digit that represents the number of measured periods.

9G-4-4. After the clock data is stored in the RAM, the P/FG counter again accumulates divided clock pulses. These pulses are not counted for the purpose of totalizing clock pulses, but rather for generating BCD codes at a constant rate. These codes, or digits, are processed decade-by-decade with the clock data stored in the RAM. The result of the process is a digitally produced frequency that is proportional to the original input period. This signal becomes F2, while the clock signal that generates the BCD codes becomes F1, hence, another period average measurement.

9G-4-5. From a theoretical standpoint, the input frequency (F_x) is used to produce average measurement ($\frac{1}{F_x}$), the data from which is used to generate a proportional frequency (F_{gen}): $\frac{1}{F_x} = P_x \propto F_{gen}$. This frequency ($F_{gen}$) is used to produce another period average measurement (P_{gen}). Since P_{gen} equals $\frac{1}{F_{gen}}$, and recalling that the generated frequency is proportional to the stored period average ($F_{gen} \propto P_x$), then the result is a frequency measurement: $P_{gen} = \frac{1}{F_{gen}} \propto \frac{1}{P_x} = F_x$.

If the actual number of periods were included, the formulas would appear as follows:

Period Average of Measured Signal: $\frac{1}{F_x} \bullet 10^n$

where 10^n = number of periods measured.

Internally generated frequency (F_{gen}): $F_{clk} \bullet \frac{1}{F_x} \bullet 10^n$

Period Average of Internal Frequency: $F_{clk} \bullet 10^5 \bullet \frac{1}{F_{gen}} = F_{clk} \bullet 10^5 \bullet \frac{1}{F_{clk} \bullet 10^n \bullet \frac{1}{F_x}} = F_x \bullet \frac{10^5}{10^n}$

The decimal point position adjusts for varying values of 10^n.

9G-4-6. Autoranging is accomplished as follows. First, the Period/Frequency Generator Counter always accumulates enough pulses during the first period average to exceed 10 percent of capacity. This ensures that all six counter decades contain data. While the period average data is being

accumulated, the Exponent Counter accumulates $\overline{\text{EXPONENT}}$ pulses from the mainframe. The number of $\overline{\text{EXPONENT}}$ pulses that occur during the period average accumulation indicates the number of positions that the decimal point must be moved in the mainframe display. The Exponent Counter data is decoded and used to drive the appropriate decimal point control line to the mainframe.

9G-4-7. A2 INPUT BOARD THEORY

9G-4-8. The input signal enters the board and passes through DC blocking capacitor C1 to input attenuator R1, R2. Capacitors C2 and C3 provide frequency compensation at the higher frequencies. With the ATTEN button out, the switch wiper connects Pins 2 and 3 of S1A, providing a direct input (X1); with the button pressed in, the switch wiper connects pins 1 and 2, selecting the attenuated signal (X100). The signal then passes through a block that provides both overvoltage protection for Q1 and switchable low pass filtering. Resistors R3 and R4 provide current limiting for clamp diodes CR1-CR4; they also provide the the R for the RC low pass filters. Capacitors C5 and C7 provide the C for the low pass filter. With neither filter selected, capacitor C4 bypasses R4 to improve high frequency performance.

9G-4-9. The first active stage is a sensitive, FET input, comparator consisting of Q1 and U1. This circuit compares the input voltage (at Q1A's gate) to a "trigger level" voltage (gate of Q1B ≈ TP1) and changes its output state when the two are equal. The "trigger level" voltage is derived from the comparator output (U1(7), TP2). This path provides the positive feedback required to make the input circuit a Schmitt trigger.

9G-4-10. The input signal is capable of swinging both positive and negative. If the counter's operation is to include the capability of triggering on either of these polarities (as selected on the front panel), the trigger level must be capable of following these voltage swings. (Recall that triggering occurs when the input voltage and the trigger level voltage are equal.) This capability is controlled by the NEG TRIG switch and is accomplished by connecting the output of U1 to a pair of supply voltages: +3.3V or -3.3V. The Schmitt trigger output (TP2) will swing from +3.3V to ground or ground to -3.3V with the NEG TRIG button pushed in. The actual trigger levels are controlled by the SENSITIVITY pot R1. This allows adjustment from minimum sensitivity (full ccw with trigger levels of ≈3V and 0V) to maximum (full cw with trigger levels of ≈6mV and 0V).

9G-4-11. Figure 9G-4-1 shows the trigger method along with the hysteresis band. Resistors R17, 18, and 15 offset the lower limits of the hysteresis band to ensure that low duty cycle pulses can cross both levels of the band.

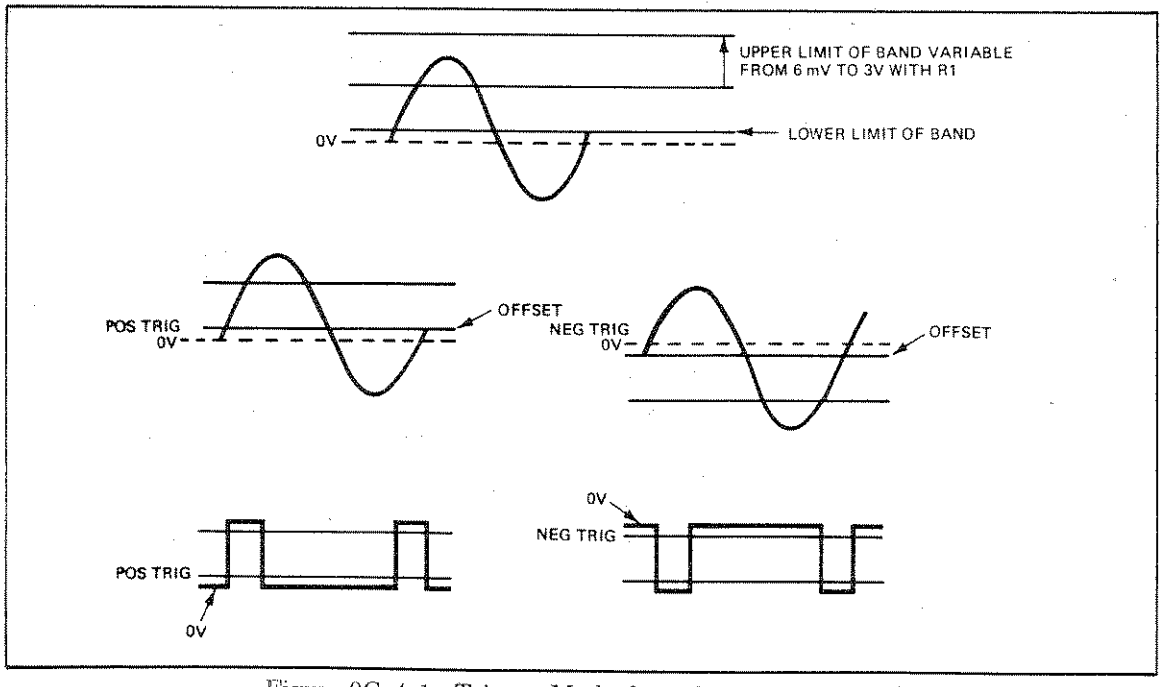


Figure 9G-4-1. Trigger Methods and Hysteresis Bands

9G-4-12. Since the output of the Schmitt trigger is not directly compatible with TTL, it is followed by level converter U2. The voltage divider of R19, 20, and 21 places +1.1V on U2(2) and -1.1V on U2(5). The output of U2 changes states when pins 3 and 6 go either above +1.1V or below -1.1V.

9G-4-13. The negative-going output of U2 feeds into a non-retriggerable one-shot, U3 (i.e., the device will not accept another input pulse until the one-shot "times out" from the first pulse). The one-shot prevents the counting of unwanted pulses. The pulse width of U3 is controlled by R26, C18, and C17. Disconnecting W1 from C17 decreases the negative pulse width.

9G-4-14. A1 LOGIC BOARD THEORY

9G-4-15. The counter has three distinct phases of operation: (1) the initial period average phase, (2) the data storage phase, and (3) the frequency generation and final period average phase. Some of the counter circuits perform different functions during the different phases; therefore, the following paragraphs describe circuit operation during each phase. Descriptions of check mode operation and CPM operation are given after the descriptions of the three standard operating phases. When reading the text, refer to the four flow diagrams at the end of this section.

9G-4-16. Initial Measurement Phase

9G-4-17. At the end the reset operation, the input signal is supplied (as the Fx signal from the A2 Input Board Assembly) to the clock input of A1U23B, the Divide-by-Two flip-flop. The output of the Divide-by-Two flip-flop is gated to the 1 MHz TIME BASE INPUT line to the 5300 mainframe, where it accumulates counts in the time base decade. The purpose of this signal, however, is not to record counts; its importance is in generating $\overline{\text{EXPONENT}}$ pulses each time the accumulation of pulses reaches a new power of ten (10^1, 10^2, 10^3, etc.). The $\overline{\text{EXPONENT}}$ pulses are totalized in U32 for determining the decimal point later in the operation. While the time base decade is accepting the Fx signal, A1U21 Clock Divider supplies 5 MHz clock pulses, through Clock Switch A1U19B, to the P/FG Counter (Period/Frequency Generator Counter, A1U1 through A1U6).

9G-4-18. When the P/FG Counter reaches 10 percent of capacity (100,000 counts), the J input of the P10 flip-flop (A1U28B) goes high. When the counter accumulates eight more counts, A1U1(12) goes from high to low and clocks the P10 flip-flop. The P/FG counter continues to count clock pulses until the next $\overline{\text{EXPONENT}}$ pulse from the 5300 mainframe clocks the PE flip-flop, A1U28A. The resulting low $\overline{Q}$ output of the PE flip-flop and the low $\overline{Q}$ output of the P10 flip-flop cause the output of gate A1U26B to go low; this inhibits the passage of Fx pulses to the 1 MHz TIME BASE INPUT line and, on the following 5 MHz clock pulse, inhibits the passage of clock pulses to the P/FG Counter. The number of input signal periods that occur while the P/FG Counter accumulates clock pulses varies with the measured input signal frequency and ranges from 2 periods to 2×10^5 periods.

9G-4-19. Data Storage Phase

9G-4-20. This phase performs two operations: It stores the clock data in a RAM, and it resets the mainframe's time base decades for the next measurement phase. Because the P/FG Counter must be used during the frequency generation and final period average phase of operation, a separate storage operation must be performed to retain the original contents of the counter. This is accomplished by using the DIGIT ADDRESS X, Y, and Z lines from the 5300 mainframe to simultaneously address the Counter Multiplexer, A1U9 through A1U12, and the storage RAM (Random Access Memory), A1U15. The DIGIT ADDRESS X, Y, and Z lines pass through the Address Multiplexer, A1U8, and are supplied directly to the RAM; gates A1U14C and A1U14D modify the code to the counter multiplexer so that P/FG Counter data is stored in reverse order, i.e., U6 data into the RAM's least-significant address location. The reason for this is discussed in subsequent paragraphs regarding the final operating phase; however, Table 9G-4-1 shows the coding for the data storage.

Table 9G-4-1. Multiplexer Codes for Data Storing Phase

DIGIT ADDRESS LINES	GENERATE THESE COUNTER MULTIPLEXER ADDRESSES	WHICH PASS DATA FROM THESE COUNTER DECADES
X Y Z	C B A	
0 0 0	1 0 1	U6
0 0 1	1 0 0	U5
0 1 0	1 1 1	U4
0 1 1	1 1 0	U3
1 0 0	0 0 1	U2
1 0 1	0 0 0	U1

9G-4-21. At the end of the original measurement phase, the Q output of the P10 flip-flop is high and the $\overline{Q}$ output of the PE flip-flop is high. These signals and the high TIME BASE OUTPUT signal line cause the TB Output Inhibit flip-flop to be set via gate A1U24C. The resulting low enable signal at A1U20D(11) allows passage of the following low TIME BASE OUTPUT pulses through A1U20D. The TIME BASE OUTPUT pulse arrives after the 5300 mainframe divides the 3.33 MHz signal on the F2 line by a factor determined by the setting of switch A1S1, which controls the TB SELECT A, B, and C signal lines. (The 3.33 MHz signal on the F2 line originates at the clock divider, A1U21, and propagates through A1U19A, A1U20A, and A1U25.) The F2 signal is used to slew the time base counter until the counter reaches maximum capacity, as determined by its enabled decade (typically the 10^5 decade). At this point, the counter contains all zeros and has, in effect, been reset.

9G-4-22. Frequency Generation and Final Period Average Phase

9G-4-23. When the time base counter has been slewed to its capacity, it outputs a low pulse on the TIME BASE OUTPUT line that clocks A1U27A. The resultant high on the Q output forces a high on A1U26C(8). This removes the low on the reset of A1U27B and allows A1U20A to pass F_{gen} to the time base counter; and, at the same time, allows A1U19B to pass 1.67 MHz to the P/FG counter. This is the beginning of the second period average.

9G-4-24. The main characteristic of the second period average is the technique used to generate a proportional frequency. This frequency is proportional to the clock data stored in the P/FG counter. As mentioned in the General Theory, the P/FG Counter again accumulates clock pulses for the purpose of generating BCD codes. These codes are multiplexed and then digitally combined (gated) with the clock data that was previously stored in the RAM. The Priority Encoder selects which multiplexer lines and RAM locations are used.

9G-4-25. The Priority Encoder, U7, produces a negative-true, octal output in compliance with the highest-priority, low-level input. The "7" input has the highest priority and will generate an LLL output, even through the other inputs may be low. If the "7" input is high and the "6" input is low, the output becomes $\frac{A_4A_2A_1}{L\ L\ H}$. Notice that the inputs are driven from the decades' CARRY OUTPUT lines. These lines are low while the decade counts from 0 to 8 and are high for the 9 count only. This means that before any specific decade can enable the Priority Encoder, all decades previous to it must be at their "9" count. For example, if U4 enables the encoder, U1, 2, and 3 must be in the 9 state, while U4, itself, must be something other than 9. Table 9G-4-2 shows the multiplexer and RAM coding for this portion of the operation.

Table 9G-4-2. Multiplexer Codes for Second Period Average

PRIORITY ENCODER OUTPUTS AND MULTIPLEXER ADDRESSES			ADDRESS CODES PASS DATA FROM	RAM ADDRESS READ AS
A_4	A_2	A_1		
L	L	L (7)	U1	0 0 0 (0)
L	L	H (6)	U2	0 0 1 (1)
L	H	L (5)	U3	0 1 0 (2)
L	H	H (4)	U4	0 1 1 (3)
H	L	L (3)	U5	1 0 0 (4)
H	L	H (2)	U6	1 0 1 (5)

9G-4-26. When the RAM stored the data from the first period average measurement, the data contained in U6 was stored in RAM location 000. Since U6 contained the most-significant-digit, it is this location that requires examination most of the time when generating the proportional frequency. This is accomplished with U1. Because U1 counts 10 times as fast as U2 and because U1 relinquishes its priority for only one count out of 10, the Priority Encoder produces a code of 7 (LLL) for the majority of time. In fact, this code addresses RAM location 000 for nine tenths of the time, while the other RAM locations must share the remaining time (see table below).

RAM LOCATION CODES

LSD					MSD	
101	100	011	010	001	000	
9×10^{-6}	9×10^{-5}	9×10^{-4}	9×100^{-3}	9/100	9/10	← Amount of Time the Address is Examined

9G-4-27. Figure 9G-4-2 shows the frequency generator as a simplified block diagram. The reference frequency of 1.67 MHz generates BCD codes from the decade counters. These codes are sent to the converting logic, where they generate waveforms 1, 2, 4, and 8. The waveforms are in the logic "1" state during one, two, four, and eight clock pulses out of 10. They are then selectively combined in the combining logic (U16) with the addressed digit from the RAM. The result is a waveform that is in the logic "1" state from 0 to 9 clock times out of 10. This waveform controls the number of clock pulses that the Pulse Gate will pass. In the example figure, the gate passes six clock pulses, which represent the 6 stored in this particular RAM location.

9G-4-28. Figure 9G-4-2 is completely factual when analyzing the circuit with regard to U1; however it is only symbolic with regard to U2 through U6. These decades can never count continually from 0 to 9 as does U1. Decade U2, for instance, is active only while U1 is at its 9 count; and, therefore, its BCD outputs are examined periodically (9 times out of 100) instead of continually.

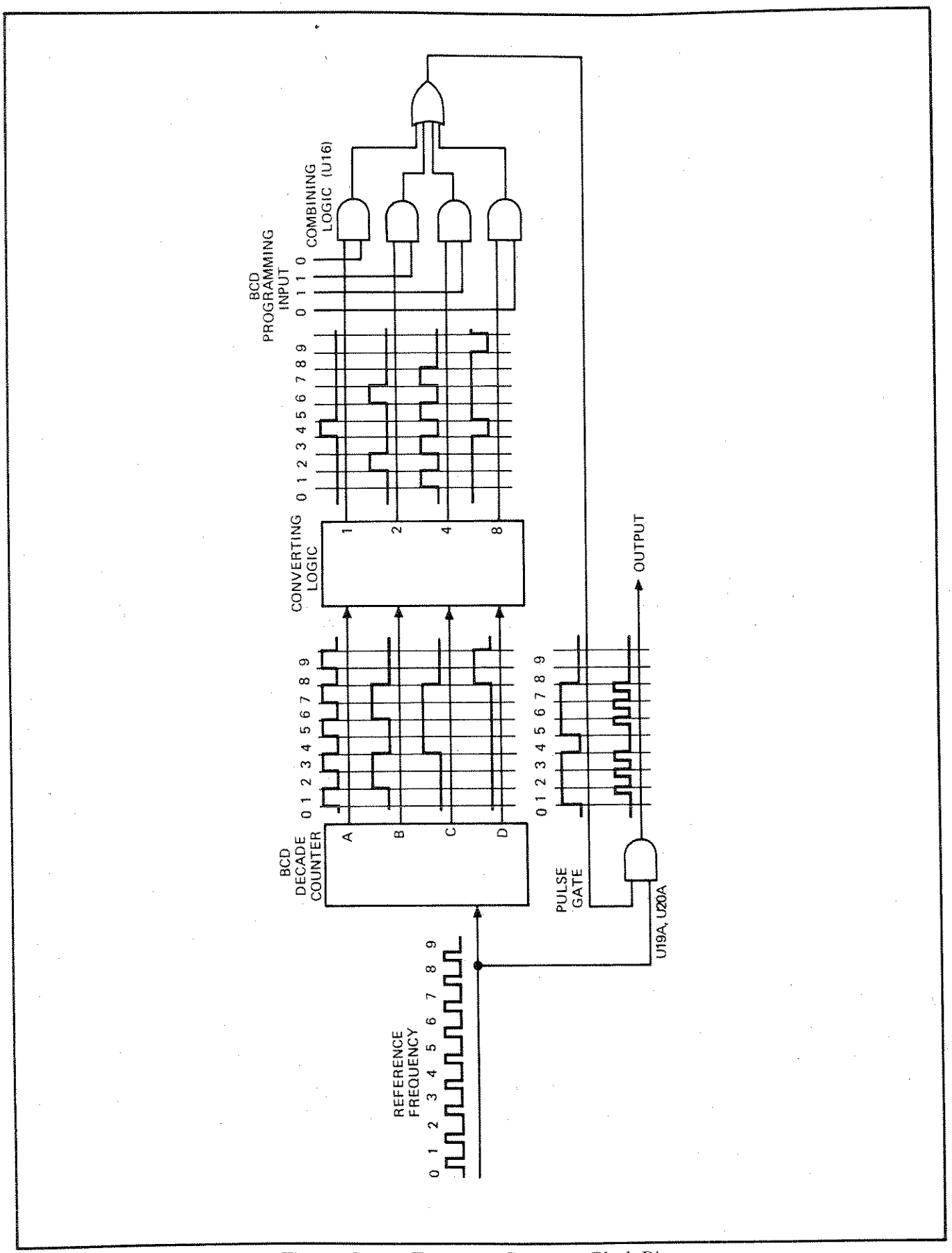


Figure 9G-4-2. Frequency Generator Block Diagram

9G-4-29. Each decade works in the same manner and is responsible for only one address location in the RAM. Remember, the digit stored in the RAM location does not change, only the BCD codes of the decade. Each decade advances through all of its states, but at a different rate than the others. Nevertheless, the effect is the same. Figure 9G-4-3 shows how a particular decade is "looked at" for only one clock pulse out of many.

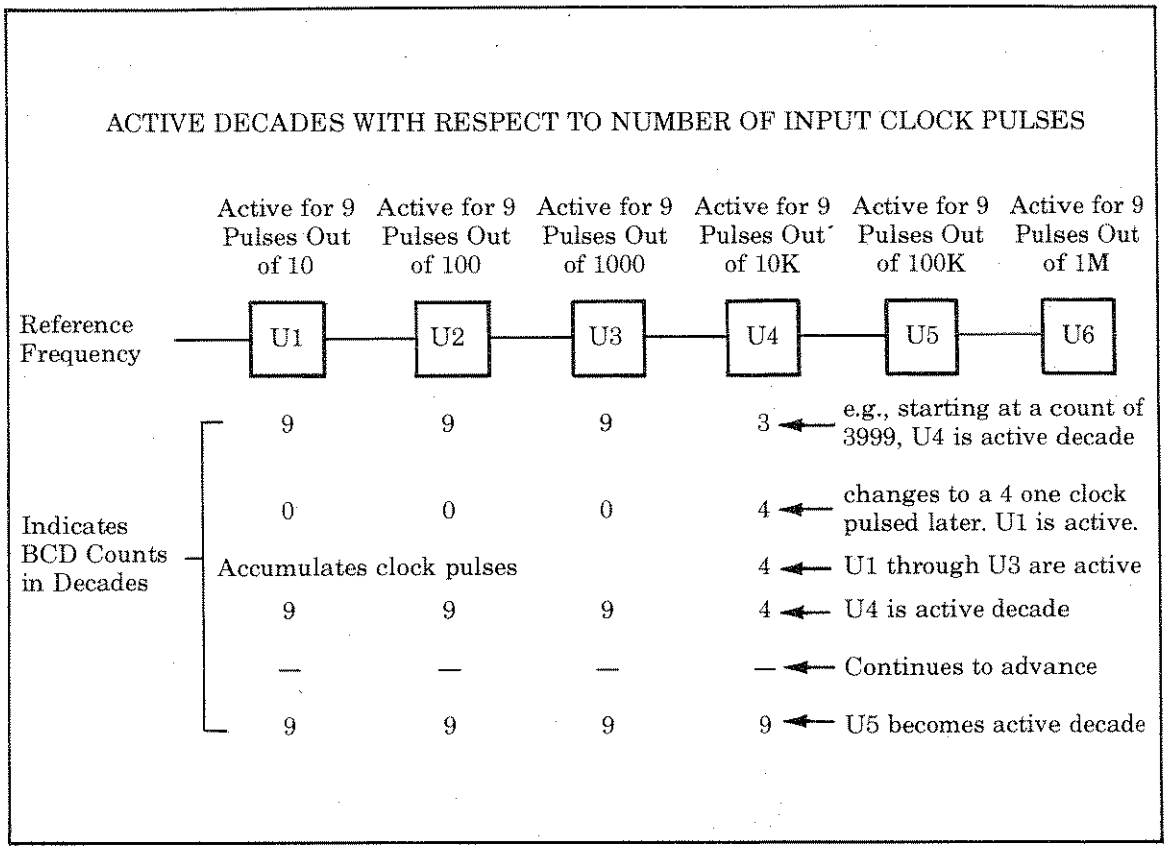


Figure 9G-4-3. Relationship of Decades to Priority Encoder

9G-4-30. The output of U16(8) is gated through U29B to U19A where it is mixed with 3.3 MHz. The signal is then mixed with 1.67 MHz in U20A and 10 MHz in U25. (The net effect being the same as if mixed with a signal having a 1.67 MHz repetition rate with 50 ns pulse width.) The resultant signal is then sent to the mainframe's Time Base decades on the F2 line. At the same time, the mainframe's counting decades receive 1.67 MHz on the F1 line from U20B and U19B.

9G-4-31. When the Time Base decades fill to their 10^5 capacity, they generate a TIME BASE OUTPUT pulse that clocks U27A via U20D. This completes the second period average measurement and the instrument's overall measurement.

9G-4-32. SELF CHECK (Hz MODE). The self check mode operates the majority of the counter's circuits with the A2 Input board being a notable exception. The counter performs a measurement in the same manner as previously described, except it substitutes 5 MHz (10 MHz clock ÷ 2) for the input signal. S2A (CHECK switch) makes contact between pins 4 and 5 to disable U22B and enable U25C. The 5 MHz clock signal enters the mainframe's Time Base decades on the F2 line instead of the 1 MHz TIME BASE line. This adds another ÷10 stage to the decade string and simulates a 1 MHz input signal for the check mode.

9G-4-33. CPM MODE. Since frequency is the number of cycles/one second, then counts per minute (cpm) would be the number of cycles/60 seconds. In a frequency measurement, the counter sends the clock signal to the P/FG counter and the input signal to the mainframe's decades. Rather than divide the clock signal by 60, as the CPM expression suggests, the 5307 divides the clock signal by 3 and multiplies the input frequency by 2. This is equivalent to dividing the clock frequency by 6. To complete the operation, the decimal point is positioned one place to the right.

9G-4-34. Electrically, these conditions are accomplished by the following methods. When the front panel switch is set to CPM, the switch (S2B) selects the D output of U21 instead of the A output. This sends 1.67 MHz (5 MHz ÷3) to the P/FG counter and accomplishes the first portion of the operation. The second part of the switch (near U32 on the schematic) places a low level on the J input of U23B and a high on the $\overline{K}$ input. This prevents U23B from dividing the input signal by two as it would in the frequency mode. Therefore, rather than actually multiplying the input signal by two, the circuit produces the same effect by eliminating a divide-by-two stage. The last phase affects the Exponent Counter, U32. In the frequency mode, this counter is reset to 9. By placing the switch wiper to pin 4, the counter resets to 0 and has the effect of shifting the decimal point one place to the right.

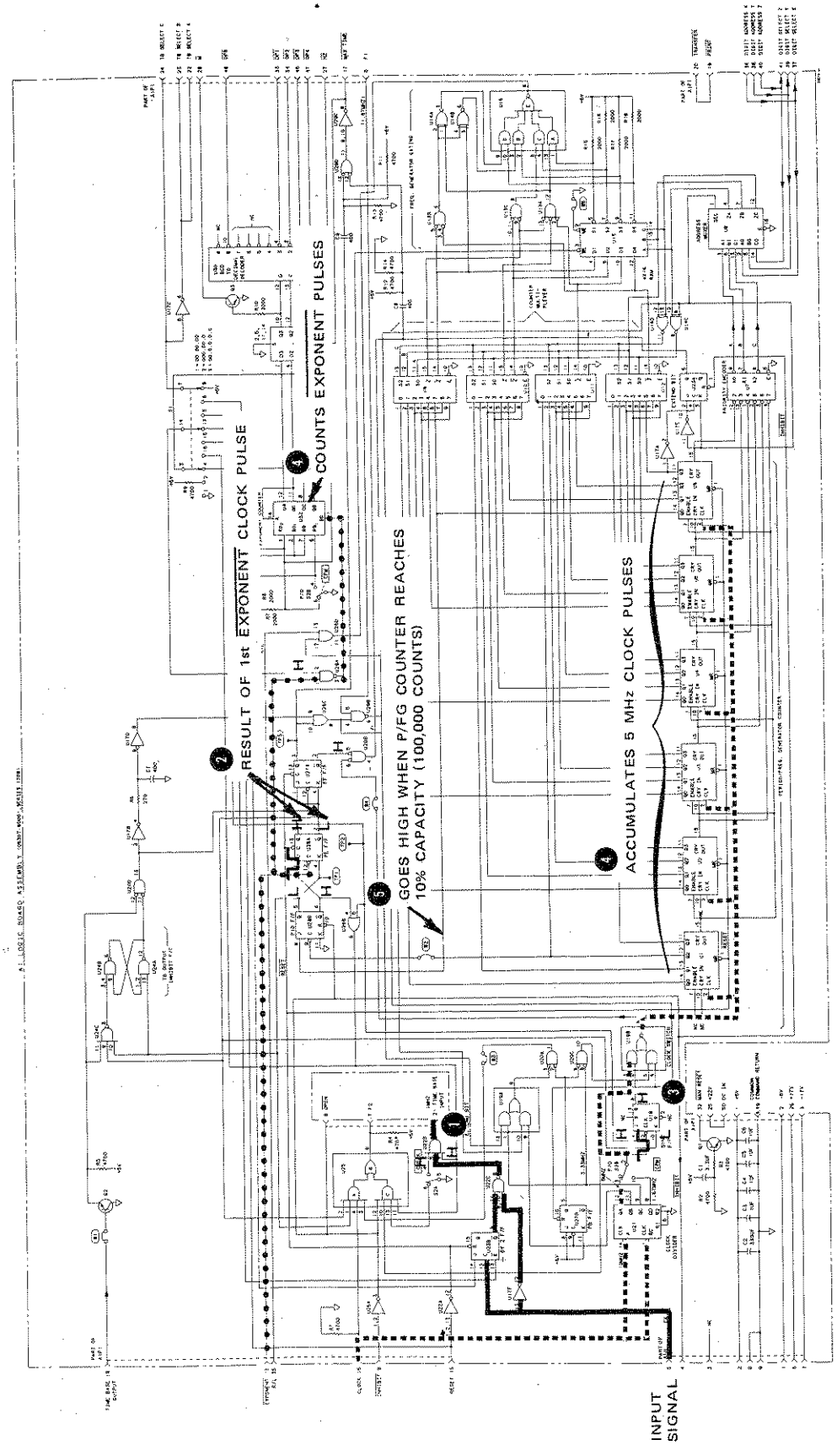


Figure 9G-4-4. First Period Average Phase

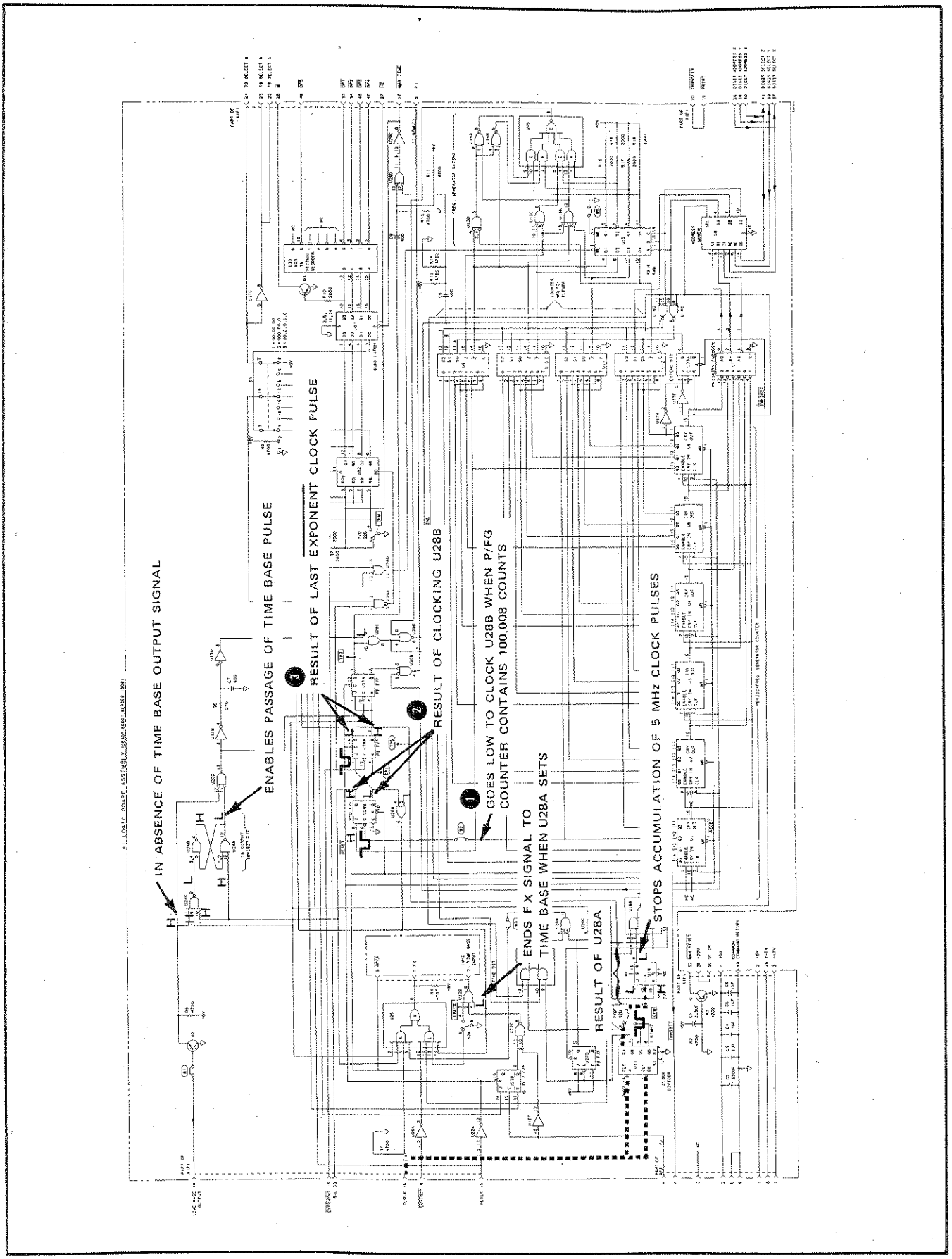


Figure 9G-4-5. End of First Period Average

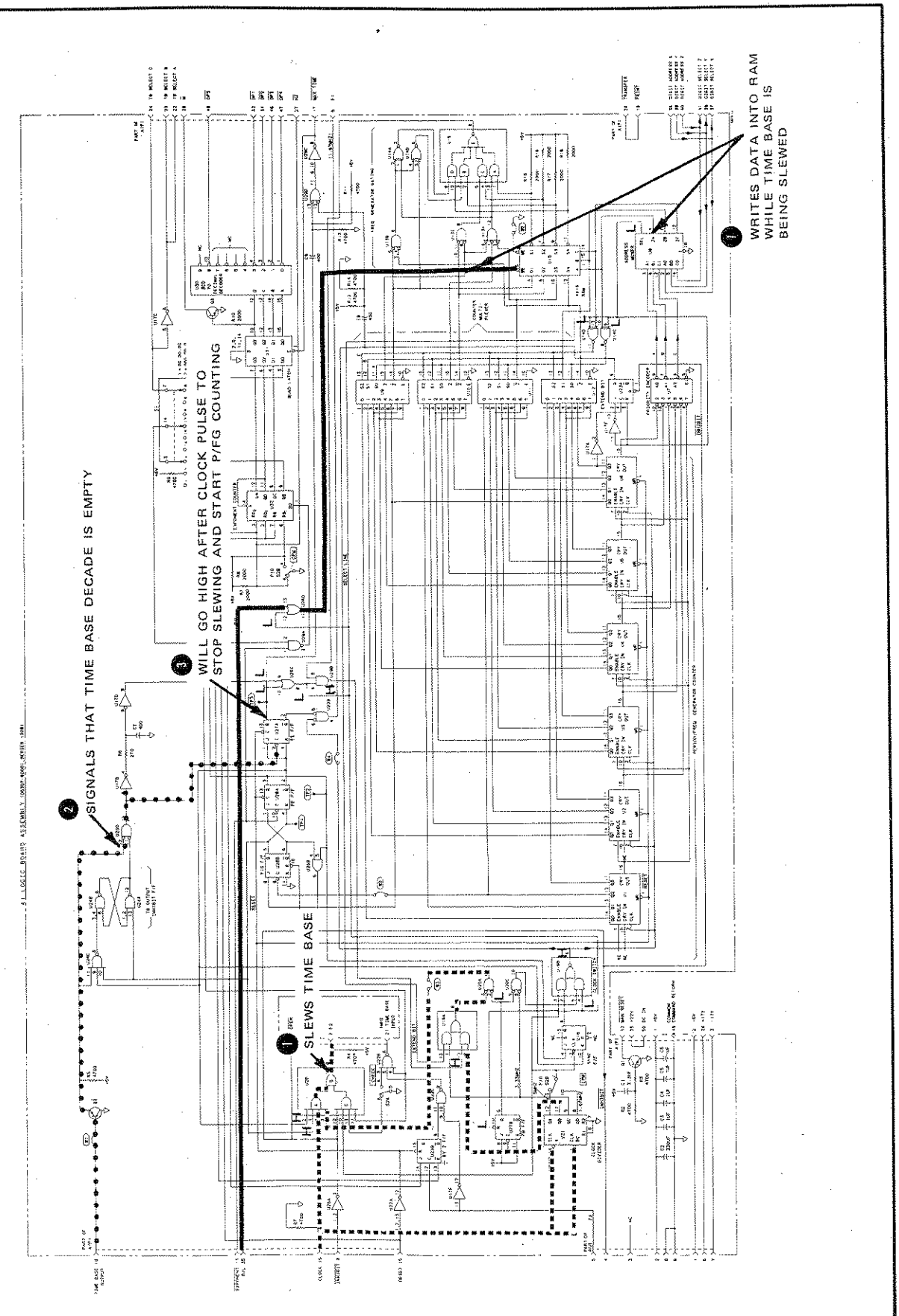


Figure 9G-4-6. Data Storing and T.B. Decade Slewing

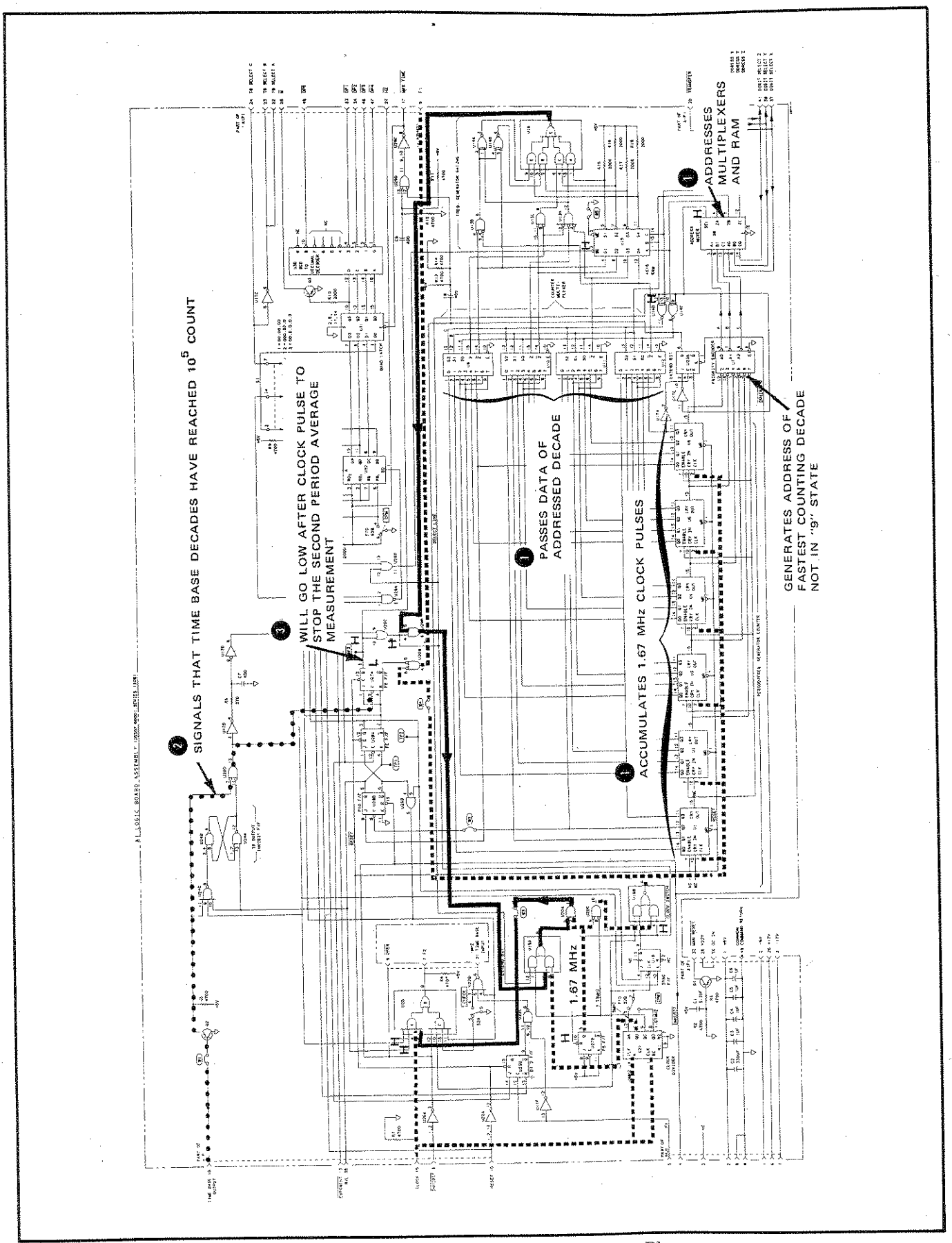


Figure 9G-4-7. Second Period Average Phase

SECTION IX G
5307A HIGH RESOLUTION COUNTER

SUBSECTION V
MAINTENANCE

9G-5-1. INTRODUCTION

9G-5-2. This subsection contains maintenance information for the counter and for the 5300 mainframe to the extent that the mainframe circuits are used by the counter. A performance check and adjustment procedures are included.

9G-5-3. RECOMMENDED TEST EQUIPMENT

9G-5-4. Test equipment recommended for proper maintenance is listed in Table 9G-5-1. Equipment with equivalent characteristics may be substituted for the recommended equipment.

9G-5-5. IN-CABINET PERFORMANCE CHECK

9G-5-6. Use the performance check in Table 9G-5-2 and the test card at the back of this subsection to verify proper operation of all the circuits in the counter. The procedure also verifies all circuits in the 5300 mainframe that are used with the counter plug-on. The performance check may be used:

a. As part of an incoming inspection check of instrument specifications.

b. Periodically, for instruments used in systems where maximum reliability is important.

c. As part of a procedure to locate defective circuits.

d. After any repairs or adjustments, before returning instrument to regular service.

9G-5-7. INSTRUMENT ACCESS

9G-5-8. For access to the plug-on assembly, separate the 5300 from the plug-on as follows:

a. Turn ac power OFF and disconnect power cord.

b. Pull the two side casting latches fully rearward while pressing the latch handles gently away from the center of the instrument.

c. When the latches are fully extended rearward, the two instrument castings will be separated by about ⅛-inch.

d. Lift the 5300 gently away from the counter.

e. Separate the counter circuit board assemblies from the cast housing as follows:

1. Press rear, plastic-nylon retaining clips on each side of the cast housing and lift the rear of the Logic Board Assembly until free from housing.

2. Release the front of the Logic Board Assembly by pressing front retaining clips and lifting front of Logic Board Assembly.

3. Lift circuit board assemblies, with front panel attached, from cast housing.

f. Connect the counter, less cast housing, to the 5300 and apply ac power.

g. To reinstall the circuit board assemblies in the cast housing, reverse procedures of steps d through f.

9G-5-9. PREVENTIVE MAINTENANCE

9G-5-10. Periodically, perform the In-Cabinet Performance Check (Table 9G-5-2) to verify proper operation. The check tests operation of both the counter and the 5300 mainframe. Additionally, check for broken or burned components, damaged connector pins, excess dust, etc., whenever the circuit board assemblies are removed from the cast instrument housing.

9G-5-11. GENERAL REPAIR

9G-5-12. The following paragraphs provide general repair information for the counter.

9G-5-13. BOARD REMOVAL. When removing the printed circuit boards for replacement, repair, or servicing, always remove ac power and separate the board from the casting according to Paragraph 9G-5-7, steps a to e.

9G-5-14. COMPONENT REPLACEMENT. When replacing a circuit board component, use a low heat soldering iron. Heat must be used sparingly as damage to the circuit foil may otherwise occur. Mounting holes may be cleaned with a toothpick while heat is applied. After component removal and replacement, clean connections with a suitable cleaning solution.

9G-5-15. INTEGRATED CIRCUIT REPLACEMENT. Two methods are recommended for removing integrated circuits:

a. Solder Gobbler. Solder is removed from board by a soldering iron with a hollow tip that is connected to a vacuum source. The IC is removed intact, so it may be reinstalled if it is later proven not to be defective.

b. Clip Out. This method is used when an IC is proven defective. Clip leads close to case, apply heat, and remove leads with long-nose pliers. Clean board holes with a toothpick and cleaning solution.

Table 9G-5-1. Recommended Test Equipment

Instrument Type	Required Characteristics	Recommended Instrument
Electronic Counter	Source of 100 kHz and 1 MHz signals with stability of better than 1 part in 10^6	HP 5245L
Function Generator	Sinusoidal output and 15% duty cycle pulses from 5 Hz to 1 MHz	HP 3310A
Oscilloscope	50 MHz bandwidth, 5 mV/cm	HP 180A/1801A/1820A
Electronic Counter/DVM	Counts frequencies to 10 MHz and has DVM	5326B
Oscillator	10 Hz to 2 MHz	651B
Synthesizer	5 Hz to 2 MHz	5103A
Logic Probe	TTL levels	10525T
Logic Pulser	TTL levels	10526T

Table 9G-5-2. In-Cabinet Performance Check

1. CHECK MODE

a. Mate the counter to a 5300 mainframe and apply ac power.

b. Press CHECK and CPM pushbuttons. Display should be 100000 M.

c. Release CPM pushbutton switch. Display should be 1.00000 MHz.

d. Release CHECK pushbutton switch.

2. ACCURACY

Obtain the following test equipment:

HP Model 5245L Electronic Counter (or other source of 100 kHz and 1 MHz signals with stability specifications as listed in Table 9G-5-1).

a. Ensure that all front-panel pushbutton switches are released (in the nonselected position).

b. Set the TIME BASE switch on the 5245L to EXT; set the rear-panel OUTPUT STD FREQ switch to 100 kHz.

c. Connect the 5245L TIME BASE EXT connector to the input terminals of the high resolution counter. Adjust the SENSITIVITY control for a stable display and observe that the display is 100000 Hz ±3 Hz.

d. Set the 5245L rear-panel OUTPUT STD FREQ switch to 1 MHz and observe that the display is 1.00000 MHz ± 0.00003 MHz.

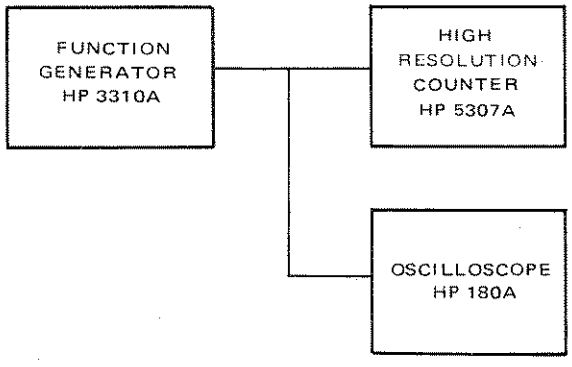
3. SENSITIVITY

Obtain the following test equipment:

HP Model 3310A Function Generator
HP Model 180A/1801A/1820A Oscilloscope

a. Ensure that all front-panel switches are released (in the nonselected position).

b. Connect the counter, the function generator, and the oscilloscope as shown below.



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d. Set the 5245L rear-panel OUTPUT STD FREQ switch to 1 MHz and observe that the display is 1.00000 MHz ± 0.00003 MHz.

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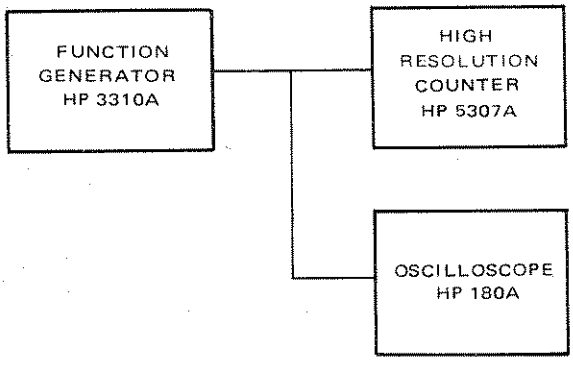
b. Connect the counter, the function generator, and the oscilloscope as shown below.



c. Rotate the counter's SENSITIVITY control fully clockwise and press the pushbutton.

d. Supply each signal listed in the table below to the counter, and observe that the counter displays each input signal at the level specified in the table. Use the oscilloscope to monitor signal levels.

e. Press the NEG TRIG pushbutton on the counter front-panel and repeat step d.

Waveshape	Signal Level	Frequency/Pulse Width
Sinusoidal	2.83 V peak-peak 2.83 V peak-peak 2.83 V peak-peak 6.07 V peak-peak	11 Hz 1100 Hz 1.1 MHz 2 MHz
⎍ Pulse (⎍ Pulse when Step e is performed)	1.5 V peak 2.5 V peak	250 ns 100 ns

4. AUTORANGING AND DISPLAY

Obtain the following test equipment:

HP Model 3310A Function Generator

a. Ensure that all front-panel pushbutton switches are released (in the nonselected position).

b. Connect the function generator to the counter INPUT terminals and supply a sine wave input of sufficient amplitude to provide a display at the following frequencies. Observe that the decimal point is positioned properly for each input frequency.

6 Hz
60 Hz
600 Hz
6 kHz
60 kHz
600 kHz
1.1 MHz

Observe that the Hz annunciator lamp lights at all frequencies and that the M annunciator lamp lights when the input frequency is 1.1 MHz.

9G-5-16. ADJUSTMENTS

9G-5-17. The counter has three adjustments: 1) amplifier balance, 2) pulse width, and 3) alternate ranging. The following paragraphs give procedures for each adjustment.

9G-5-18. Amplifier Balance Adjustment

9G-5-19. The amplifier balance adjustment is set at the factory and rarely needs readjustment. If components within the amplifier circuits are replaced, however, readjust the balance as follows:

a. Remove the circuit board assemblies from the instrument's cast housing as described in Paragraph 9G-5-7.

b. Remove the three machine screws that hold the A2 Input Board Assembly to the threaded spacers on the A1 Logic Board Assembly.

c. Gently lift the rear of the A2 Input Board Assembly to disconnect the inter-board connector (A1J1-A2P1), and remove the A2 assembly with the front panel attached.

d. Remove the three machine screws that attach the sheet metal cover on the component side of the A2 Input Board Assembly and remove the cover. When reassembling cover, ensure that the cable from the SENSITIVITY control is routed on the outside of the cover and that the cable does not come in contact with the front-panel switch mechanisms.

CAUTION

IN THE FOLLOWING STEP, BE SURE TO ALIGN THE TWO CIRCUIT-BOARD CONNECTORS PROPERLY. DAMAGE TO THE INSTRUMENT MAY OTHERWISE OCCUR.

e. Interconnect the circuit-board assemblies as illustrated in Figure 9G-5-1 and mate the two assemblies to a 5300 mainframe.

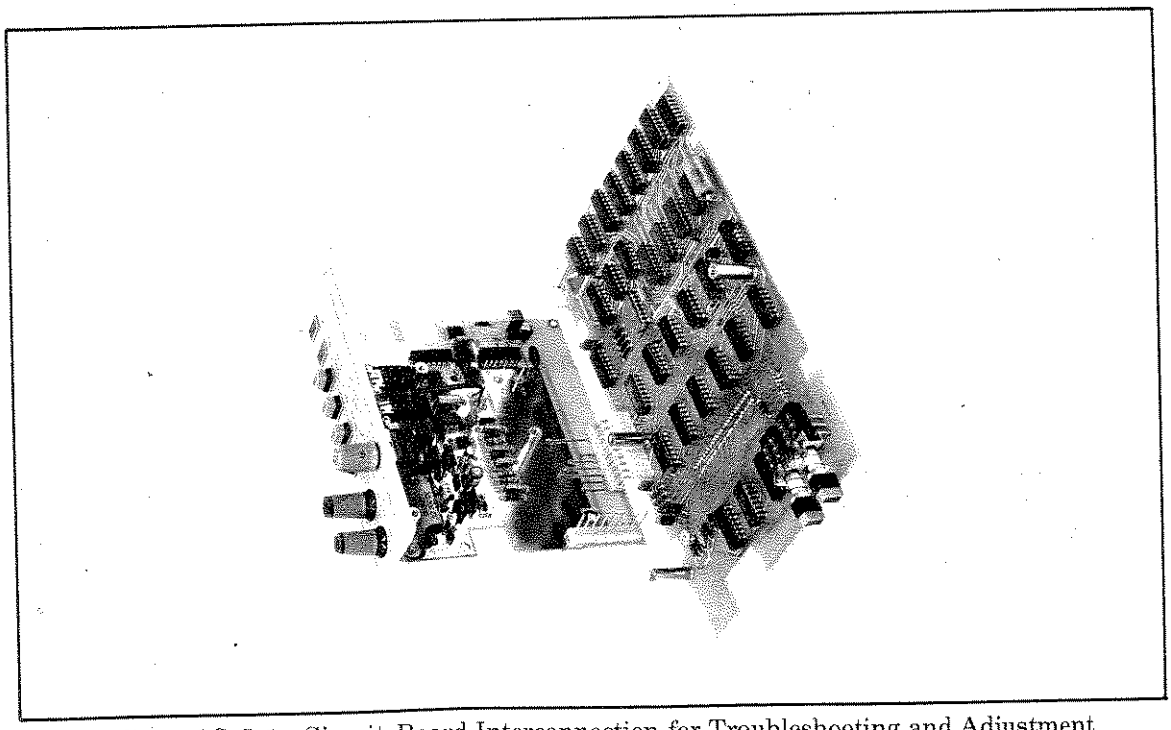


Figure 9G-5-1. Circuit-Board Interconnection for Troubleshooting and Adjustment

f. Apply ac power and monitor A2TP2 with an oscilloscope.

g. Short A2TP1 to the circuit board common return line (ground potential) with a short clip-lead.

h. Adjust A2R7 in each direction and note the range of adjustment over which oscillation is observable on the oscilloscope. Set A2R7 to the center of this range. (This point also corresponds to the highest frequency of oscillation.)

i. Remove test equipment and reassembly the counter in reverse order of disassembly.

9G-5-20. Pulse Width Adjustment

9G-5-21. The Pulse Width adjustment sets the time that the counter circuits are inhibited after triggering on an input pulse (refer to Paragraph 9G-3-10, Count Holdoff Capability). Set the Pulse Width to eliminate undesired triggering as follows:

a. Perform steps a through e in Paragraph 9G-5-19.

b. Apply ac power to the counter/mainframe.

c. Set jumper A2W1 to position A (or 1 if board is so labelled) if a pulse width of approximately 5 μsec to 0.5 μsec is desired (this allows A2R26 to be adjusted to limit the maximum repetition rate of input pulses to any value between approximately 200,000 pulses per second and 2,000,000 pulses per second). Set jumper A2W1 to position B (or 2 if board is so labelled) if a pulse width of 10 msec to 1 msec is desired (this allows A2R26 to be adjusted to limit the input pulses to approximately 100 pulses per second to 1000 pulses per second.

d. If the desired pulse width is known, monitor A2TP4 with an oscilloscope, apply an input signal to the counter, and adjust A2R26 until the low level of the signal at A2TP4 is the desired width.

e. If the desired pulse width is not known, connect the signal to be measured to the counter INPUT terminals and observe the mainframe display. If the display is a multiple of the known input frequency turn A2R26 counterclockwise until the display is correct. This lengthens the pulse width and inhibits multiple triggering on a ringing signal or other complex signal. If the display shows that the input signal is divided in the counter circuits, turn A2R26 clockwise until the display is correct.

NOTE

To perform the above step, it may be necessary to observe the complex input waveform on an oscilloscope to determine the approximate frequency of each pulse group.

f. Reassemble the counter in reverse order of disassembly.

9G-5-22. Alternate Ranging Adjustment

9G-5-23. The alternate ranging adjustment is made with a three-position switch (A1S1) that is located on the back side of the A1 Logic Board Assembly. In the normal position (labelled 00.0.0.0.0. on the printed-circuit board), autoranging occurs in decade steps. If a measured signal varies above and below an autoranging point, it may be desirable to suppress alternate auto-

ranging points. Remove the counter from the mainframe according to Paragraph 9G-5-8, steps a through d. Place switch A1S1 to the position marked "000.00.0" to suppress the even-numbered autoranging points; place the switch to the position marked "00.00.00." to suppress the odd-numbered autoranging points.

NOTE

Counter operation is affected by A1S1 setting

WITH 5300A

Front Position:	Hz - Counter operates properly CPM - decimal points and annunciators are correct below 10μ CPM
Middle Position:	Hz - at 100 kHz and above, counter will not light decimal point. CPM - at 100K CPM and above, counter will not light decimal point.
Rear Position:	Hz - counter operates properly CPM - decimal points and annunciators are correct below 10μ CPM

WITH 5300B

Front Position:	Hz - counter operates properly CPM - decimal points and annunciators are correct below 10μ CPM

9G-5-24. INSTRUMENT TROUBLESHOOTING

9G-5-25. The following troubleshooting procedure is strictly concerned with problems associated with the A1 Logic board. Should the A2 Input board be suspect, refer to the waveforms next to the schematic. The following troubleshooting information is divided into 4 general headings:

1. Special Symptoms
2. Counter Does Not Cycle
3. Counter Cycles, No Display
4. Inaccurate Display.

NOTE

Always read Special Symptoms before beginning any troubleshooting

9G-5-26. Special Symptoms

Symptoms are Frequency Dependent — Depending on the input frequency used, counter may have symptoms of 1) counter does not cycle, no display, 2) counter cycles, displays incorrect answer with overflow (OF) light.

The problem lies in the Frequency Generator part of the circuit. Set the input frequency to give an incorrect reading on the display and perform the troubleshooting procedure outlined under INACCURATE DISPLAY.

Display Reads 16667 — Counter cycles and reads 16667 with any input frequency. Time Base decades are receiving 10 MHz only and not the signal from U20(1). Check that U19B(8) is toggling and that signal is present at U20A(1).

Display Reads 100000 — Counter cycles, U16 pin 8 is being held low.

Incorrect Display, Single Cycle, OF Light — Must push RESET before counter can make measurement. Problem is in MAX TIME circuit, U29C and D. $\overline{\text{MAX TIME}}$ line is being held high.

Incorrect Count at V.L.F. — Counter cycles but displays incorrect frequency with input of 7 Hz. Extend Bit output at U23A pin 6 is not going high or U19A is not passing 3.33 MHz at this time (U19A pin 13 should be toggling high to pass the 3.33 MHz signal).

9G-5-27. Counter Does Not Cycle

9G-5-28. This troubleshooting procedure is specifically for counters having symptoms of (a) no display (other than zeros) and (b) count light does not flash. The procedure is divided into 2 parts: Part A and Part B. The test immediately following will determine which one should be used.

TEST: Connect 900 kHz to input jack. Place logic probe on TP1 and hold RESET button in. Logic probe should indicate a low level. Release button; probe should indicate a high. If high, continue troubleshooting using PART A. If TP1 remains low, use PART B.

PART A. A high at TP1 indicates that:

a. The input signal is going to the mainframe's time base decades.

b. An $\overline{\text{EXPONENT}}$ pulse clocked U28A, which allows clock pulses to enter the P/FG counter.

c. The P/FG counter and U28B are working.

TEST STEPS:

1. Place logic probe on U29C(8). The $\overline{\text{MAX TIME}}$ line should be high; if not, check U29C and D (pins 13 and 12 should be high).

2. Hold RESET button in. Place logic probe on U25 pin 8 (the F2 line). Release button; probe light should begin flashing. If not, check that U20A pin 1 is not being held low. If U20A pin 1 is low, hold RESET button in while checking this pin. Probe light should begin flashing. If it does, check for Fgen at U16(8) using an oscilloscope. If probe light does not flash, check U20A and U19A.

3. Hold RESET button in. Place logic probe on U27A(12). Release button; probe should flash. If not, check the TB OUTPUT INHIBIT F/F circuit is allowing time base pulses to pass through U20D. U28 pins 5 and 2 should now be high. Also, ensure U27A pin 12 is not shorted to ground.

4. Hold RESET button in. Place logic probe on TP3. Release button; probe should go from low to high. If not, U27A is bad or the gates on its outputs are preventing it from setting.

PART B

TEST STEPS:

1. Hold RESET button in. Place logic probe on U22B(6) to check for presence of signal. Release button; probe should begin flashing. If not, check for a high level on U22B(4) and the presence of signal on pin 5.

2. Hold RESET button in. Place logic probe on TP2. Release button; probe should indicate a high level. if not, check that:

   a. U28A pin 1 is high.
   b. U28A pin 12 is not shorted to ground.

3. Place logic probe on U19B(6). Probe light should flash indicating presence of clock signal. If not, retrace clock signal through U18 and U21. U19B pin 2 should be high with clock signal on pin 3.

4. The presence of a signal at U19B(6) indicates that the failure is in the P/FG counter. The P/FG counter would be rendered inoperative if the Priority Encoder, U7, or the Counter Multiplexers, U9-U12, were shorted to ground. Check the CARRY OUTPUT of each decade (U1-U6) until the faulty one is detected.

9G-5-29. Counter Cycles, No Display

9G-5-30. This troubleshooting procedure is specifically for counters having symptoms of (a) no display (other than zeros) and (b) the count light flashes.

Connect 900 kHz to the input jack and check the following points, using a 10525T Logic Probe.

TEST STEPS:

1. Place logic probe on TP1. Push RESET button once. Probe light should begin flashing. If not, check that U28 pins 8, 9, and 10 are toggling before replacing U28. Also, any circuit on U28's output that is shorted to ground would prevent the F-F from toggling.

2. Check for F1 signal at U20 pin 4. If probe does not flash, check that U26C(8) is high and that the 1.67 MHz signal is passing through U19B (use oscilloscope). The 5 MHz signal from the first period average will alternately appear at U19B(6) as the counter cycles.

9G-5-31. Inaccurate Display

9G-5-32. This portion of the troubleshooting section pertains to counters that perform a measurement, but whose readings are incorrect. These problems will typically occur in the P/FG counter or in the Frequency Generator circuit. Since the procedure to locate problems in this area is extensive, check for your counter's symptoms under **Special Symptoms** before beginning. Also, it is important that it be understood what is and what is not an incorrect display.

9G-5-33. Part of the counter's accuracy specification (see Table 9G-1-1) is the internal frequency generator's inherent error (worst case) of $\pm 3 \times 10^{-5}$. This means that with a 2 MHz input signal an error of 60 Hz could exist without regard to the other portion of the accuracy specification. The resultant display could be anything within the range of 2.00006 MHz to 1.99994 MHz. Using 900 kHz could result in an error of 27 Hz and the counter could display 900027 Hz to 899973 Hz. Again, this is without regard to the remainder of the specification. To determine this error, simply multiply the input frequency times 3×10^{-5}, e.g., $9 \times 10^{5} \times 3 \times 10^{-5} = 27$. At these higher frequencies, the trigger error becomes relatively insignificant.

9G-5-34. The ±1 count error associated with most electronic counters is included in the $\pm 3 \times 10^{5}$ error. In most frequency counters, the ±1 count error refers to a one count error in the display's least-significant-digit. However, this is not the case in the 5307, since this counter performs a frequency measurement by making period average measurements. At the end of the first period average measurement, the P/FG counter contains a number equal to the first six digits of $\frac{1}{F_{in}}$. If the input signal were 900 kHz, each decade would contain a count of one (111111) at the end of the first Period average measurement ($\frac{1}{900\ K} = 111111$). If the P/FG counter were off by one clock pulse, it would affect the display in the reverse manner ($\frac{1}{111110} = 900009$). This explains the "1" that occurs intermittently in the display's second column (900010 Hz) when measuring 900 kHz.

9G-5-35. Display inaccuracies resulting from trigger error of the input signal are most apparent at the lower frequencies. At 60 Hz, for example, the display may appear slightly erratic in the less-significant digits and yet be well within specifications. Note: The 100 Hz low pass filter should be used when measuring 60 Hz. The trigger error is "less than ±.03% of one period ÷ periods averaged for sine waves with 40 dB or better signal to noise ratio." The table below lists the number of periods averaged for a given input signal.

Input Signal (Hz)	Periods Averaged
5–100	2
100–1k	20
1k–10k	200
10k–100k	2k
100k–1M	20k
1M–2M	200k

Example, using 60 Hz: $\frac{\pm 3 \times 10^{-4} \times 0.1666}{2} = \pm 2.5 \times 10^{-5}$

This error could, in itself, result in a display of 60.0025 Hz or 59.9975 Hz.

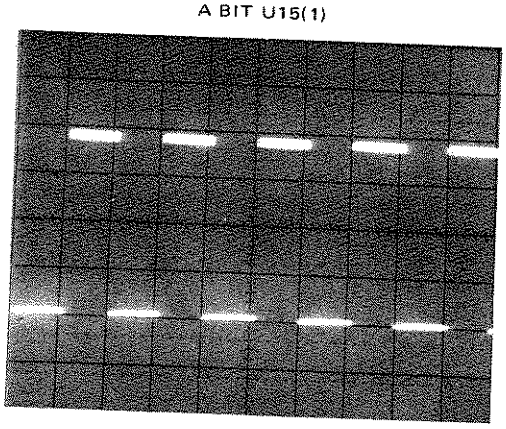
9G–5–36. TROUBLESHOOTING AN INACCURATE DISPLAY. The following troubleshooting procedure is directed to the A1 Logic board. *Before beginning this procedure, check waveform number 2 shown under A2 troubleshooting to ensure the A2 board is operating properly.*

9G–5–37. Select the input frequency that causes an incorrrect display, preferably one above 60 Hz. If using a synthesizer, try 213555 Hz, since this frequency is used in the examples that follow.

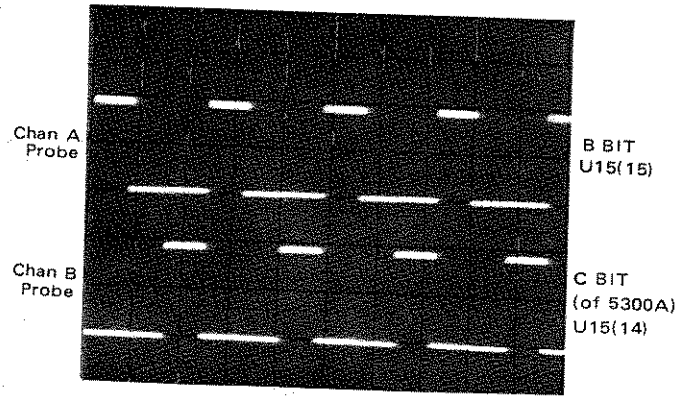
TEST STEPS:

1. Place a logic probe on U26C(9) Push RESET button once. Probe light should begin flashing. If not, check circuit of U17B and D.

2. Remove the input signal and check the three output lines of U8 with an oscilloscope using an AP clip. U8 pin 1 should be low to allow the DIGIT ADDRESS codes to appear on the output lines. See waveforms shown below. **Also**, check that the "A" and "C" bits are inverted at U14(8) and U14(11), respectively.



10:1 divider probe
.1V/Div, .2ms/div
TRIGGER - NEG SLOPE



10:1 divider probe
.2V/Div, .5ms/div
TRIGGER - NEG SLOPE

3. Connect the input signal, once again, and lift W2. Push RESET button once. Use oscilloscope to check that signal on U1(2) is actually 5 MHz (period is .2 μs).

4. Reconnect W2 and lift W1. Push RESET button once.

5. Place logic pulser on U27A(12) and pulse it once. This allows 1.667 MHz to enter the P/FG counter. Use oscilloscope on U1(2) to check that signal is actually 1.67 MHz (period should be .6 μs). The outputs of U8 should now be generated by the Priority Encoder, U7. Check that U14C and D are *not* inverting the A and C bits of U8. (Increase oscilloscope intensity.) Pulses will appear different than when checked previously.

6. Connect the BNC end of the 10:1 oscilloscope probe to the Channel A input jack of the 5326B. Set the gate time to 10 seconds and adjust the trigger level to read +.15V. The table below indicates the proper frequencies to be measured on U15.

U15 Pin #	Frequency
1	151.516 kHz
15	16.5016 kHz ±1
14	.1666 kHz

If the measured frequencies differ from those listed above, the problem is in the P/FG counter or the Priority Encoder. To check the P/FG counter, measure the frequency at pin 15 of U1 through U6 to ensure that the decades are dividing the 1.667 MHz signal by 10. The readings should be as shown in the table below. Replace any decade that is not dividing properly.

Pin 15 of IC	Gate Time	Counter Reading
U1	.1s	166.66 KHz
U2	1s	16.666 KHz
U3	1s	1.666 KHz
Switch Counter to Period Mode		
U4	1 μs	6000 μs
U5	10 μs	60000 μs
U6	10 μs	600.00 ms

The remainder of this procedure tests the accuracy of the decade's BCD outputs and checks that the data is being properly addressed through the counter multiplexer and RAM.

NOTE

There are two step 7's. One uses a synthesizer and the other lists a 651B oscillator as an alternative. Perform only one of these steps.

FOR SYNTHESIZER ONLY

7. As described previously, select the synthesizer's frequency that causes an incorrect display. Again, try 213,555 Hz since this frequency is used in the following examples. Lift W1 and push RESET. The clock data should now be stored in the decades. Using a calculator, take the reciprocal of the input frequency. For example, if the frequency is 213555 Hz, the answer is $\frac{1}{213555} = 468263$. This is the number that should be stored in the decades with the most-significant-digit (4) being stored in U6. *Write this number down, since it will be referred to later.*

   Using a logic probe, check the BCD outputs of each decade (U1-U6) and compare it to the calculated number. For this example, the number should appear as in the table below. If the number in U1 is off by one count, push the RESET button a few times until the proper number appears.

IC	PINS 11	12	13	14	Decimal
U1	0	0	1	1	3 (±1 count)
U2	0	1	1	0	6
U3	0	0	1	0	2
U4	1	0	0	0	8
U5	0	1	1	0	6
U6	0	1	0	0	4

If one of the numbers is incorrect, double check the BCD code and your conversion from BCD to decimal before replacing the IC.

END OF STEP 7 FOR SYNTHESIZER

FOR 651B ONLY

7. When using a 651B, it cannot be accurately determined what number will be stored in the P/FG counter after the first period average. Therefore, to check that the BCD outputs of the decades are working properly, a dynamic check is needed.

   a. Reconnect W1 and lift W2. Push RESET once.

   b. Perform a time interval measurement on the decade output lines by setting the 5326B counter controls as shown below and comparing the readings with those shown in the table. Use a 10:1 probe and set the trigger levels of both channels to +.15V.

5326B controls set as follows:

FUNCTION ..... T.I. A to B
TIME BASE ..... .1 μs
CHANNEL A
  SLOPE ..... +
  Coupling ..... DC
  ATTEN X1
CHANNEL B
  SLOPE ..... –
  Coupling ..... DC
  ATTEN X1
CHK-SEP-COM ..... COM

DECADE	COUNTER DISPLAY			
	Pin 14	Pin 13	Pin 12	Pin 11
U1	.2 μs	.4 μs	.8 μs	.4 μs
U2	2.0 μs	4.0 μs	8.0 μs	4.0 μs
U3	20.0 μs	40.0 μ	80.0 μs	40.0 μs
U4	200.0 μs	400.0 μs	800.0 μs	400.0 μs
U5	2000.0 μs	4000.0 μs	8000.0 μs	4000.0 μs
U6	20000.0 μs	40000.0 μs	80000.0 μs	40000.0 μs

Replace any IC whose readings differ from those listed.

   c. Reconnect W2 and lift W1. Push RESET once.

   A separate number is now stored in each decade of the P/FG counter. Using a logic probe, check the BCD outputs of each decade (U1–U6) and record the number: it will be used later in the procedure.

Example

IC	PINS				Decimal
	11	12	13	14	
U1	0	1	0	1	5
U2	1	0	0	0	8
U3	0	1	1	0	6
U4	0	0	1	1	3
U5	0	1	0	0	4
U6	0	1	1	1	7

END OF STEP 7 FOR 651B

8. The next step is to ensure that the data stored in the decades can be written into the RAM correctly and can be read from the RAM correctly. Using two 10:1 divider probes, connect the Channel B probe to U15(14). An AP clip on U15 is helpful. (W1 should now be lifted.)

   a. Set the oscilloscope controls as follows:

VOLTS/DIV (both channels)	.2V/DIV
TIME/DIV	.1ms/DIV
DISPLAY	CHOP
POLARITY (both channels)	POS
TRIGGER	AUTO
TRIGGER POLARITY	NEG SLOPE

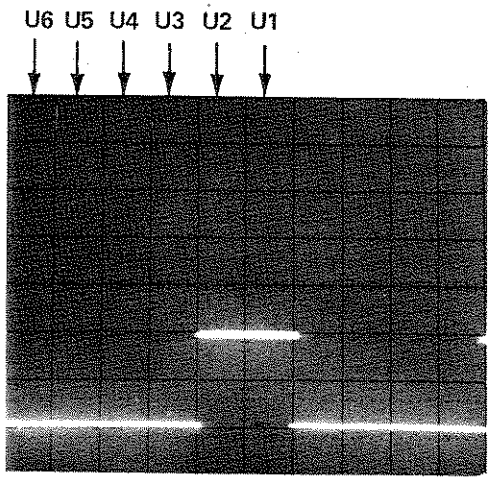
   b. Use the TIME/DIV VERNIER knob and the HORIZONTAL knob to adjust the pulse's width and position. The controls should be adjusted so the waveform appears like that shown in one of the photos below. (The pulse width depends on the mainframe used: 5300A or 5300B.)

      5300A: Set the pulse so that its positive-going and negative-going edges cover the two center graticule lines.

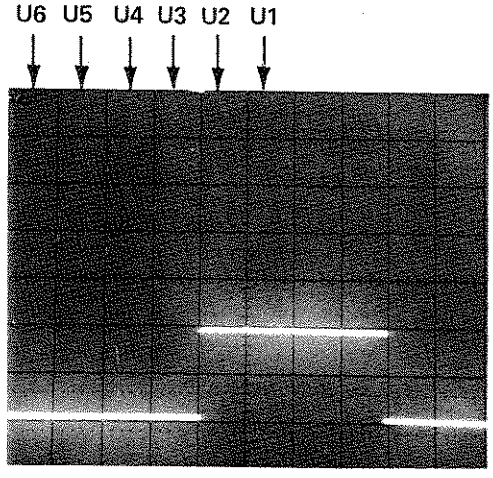
      5300B: Set the pulse so that its positive-going edge occurs on the 4th vertical line from the left and the negative-going edge occurs on the 2nd vertical line from the right.

This sets up six columns (between graticule lines) starting from the left and ending six lines from the left. The six columns represent each of the six P/FG decades with U6 being on the left and U1 being 6 columns to the right. Ignore any pulses to the right of this point.

5300A



5300B

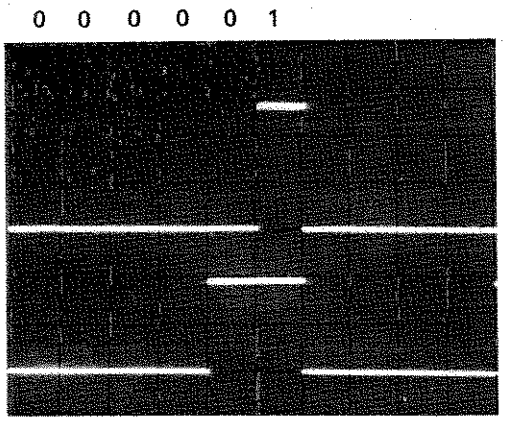


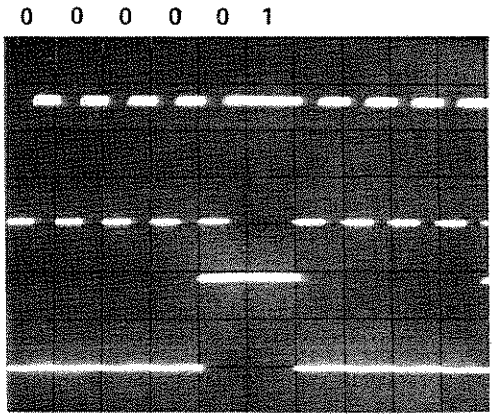
NOTE

The difference in waveforms shown below is due to differences between manufacturers of U15. They are read in the same manner, however. In the photos on the right, the right side of each column will always be high. Therefore, if the left side of a column is low, the bit for that decade is 0.

c. Place the Channel A probe on U15 pin 5; the oscilloscope will show the "A" bit of each decade. Write these down in BCD form. In this example:

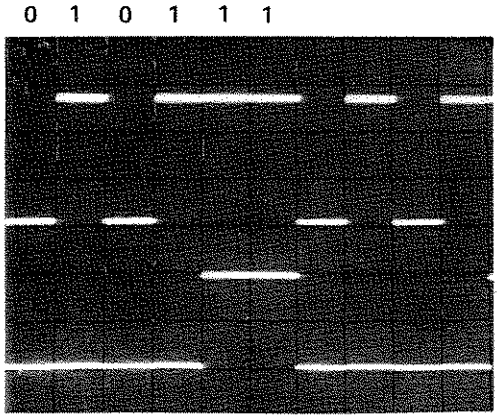
U6 DCBA	U5 DCBA	U4 DCBA	U3 DCBA	U2 DCBA	U1 DCBA
0	0	0	0	0	1

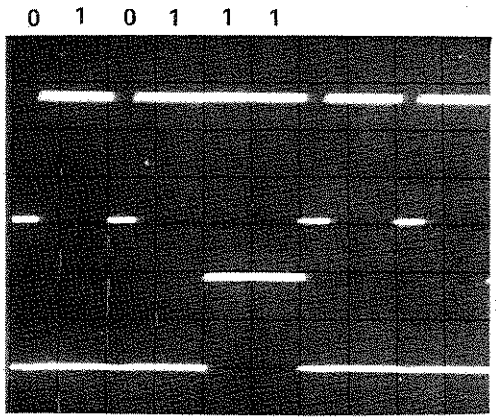




d. Next, move the Channel A probe to U15 pin 7 and check the "B" bit of each decade. Record it as shown below.

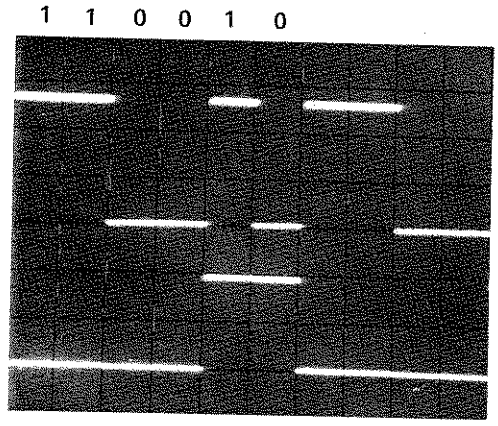
U6 DCBA	U5 DCBA	U4 DCBA	U3 DCBA	U2 DCBA	U1 DCBA
00	10	00	10	10	11

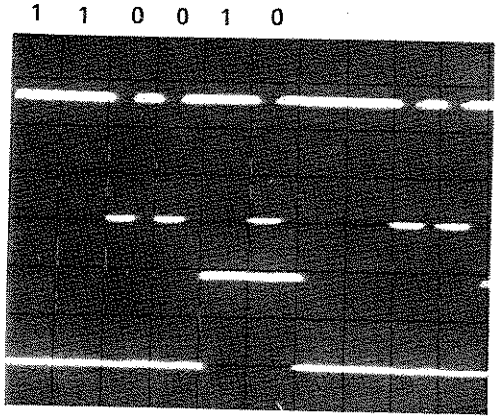




e. Then record the "C" bit at U15 pin 9.

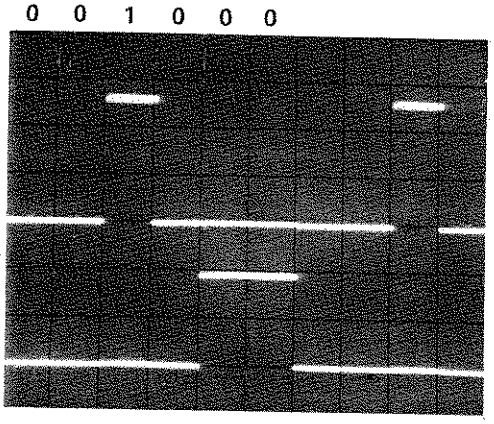
U6 DCBA	U5 DCBA	U4 DCBA	U3 DCBA	U2 DCBA	U1 DCBA
100	110	000	010	110	011

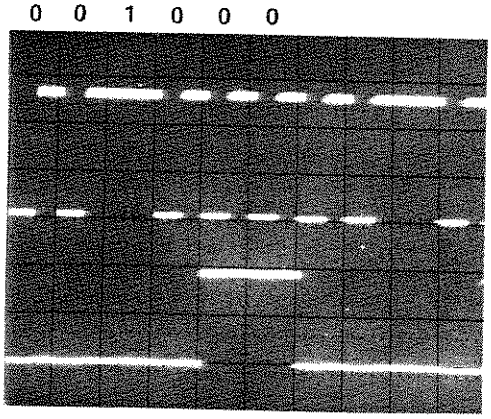




f. Finally, record the "D" bit at U15 pin 11, and convert the BCD number to its decimal equivalent.

U6 DCBA	U5 DCBA	U4 DCBA	U3 DCBA	U2 DCBA	U1 DCBA
0100	0110	1000	0010	0110	0011
4	6	8	2	6	3





g. This should be the same number that was checked in step 7 with a logic probe. If it is not the same number, the problem is in the RAM or the multiplexer. To determine which one, change the POLARITY switch of Channel A to the NEG position and repeat this procedure, this time checking the inputs of the RAM. If the number here is the number that was stored in the decades, replace the RAM. Otherwise, the problem is in the multiplexer that transferred the wrong bit.

9. If the RAM's outputs were correct, leave the POLARITY switch in its POS position and check the Z outputs of U9 and U10 in the same manner that the RAM outputs were checked. If the Z outputs are identical to the previously checked A and B bits, the problem lies in U13, U14, or U16.

10. Replace W1 and push RESET. Using a logic probe, check the outputs of U13 and U14 to determine if they are capable of toggling. If so, replace U16.

SECTION IX G
5307A HIGH RESOLUTION COUNTER

SUBSECTION VI
REPLACEABLE PARTS

9G-6-1. INTRODUCTION

9G-6-2. This subsection contains information for ordering replacement parts. Table 9G-6-1 lists parts in alphanumeric order of reference designations and provides the following information on each part: 1. Hewlett-Packard part number, b. description of part (see abbreviations below), c. total quantity used in the instrument (the total quantity appears after the first entry for a given part), d. typical manufacturer of the part in a five-digit code (see list of manufacturer's in Table 9G-6-2), e. manufacturer's part number.

9G-6-3. Miscellaneous parts are listed at the end of Table 9G-6-1.

9G-6-4. ORDERING INFORMATION

9G-6-5. To obtain replacement parts, address order to your local Hewlett-Packard Sales and Service office (see lists in Section VI of the 5300A manual for addresses). Identify part by their Hewlett-Packard part number. To obtain a part that is not listed, include:

a. Instrument model number.
b. Instrument serial number.
c. Description of the part.
d. Function and location of the part.

REFERENCE DESIGNATORS

A	assembly	F	fuse	MP	mechanical part	U	integrated circuit
B	motor	FL	filter	P	plug	V	vacuum, tube, neon bulb, photocell, etc.
BT	battery	IC	integrated circuit	Q	transistor		
C	capacitor	J	jack	R	resistor	VR	voltage regulator
CP	coupler	K	relay	RT	thermistor	W	cable
CR	diode	L	inductor	S	switch	X	socket
DL	delay line	LS	loud speaker	T	transformer	Y	crystal
DS	device signaling (lamp)	M	meter	TB	terminal board	Z	tuned cavity, network
E	misc electronic part	MK	microphone	TP	test point		

ABBREVIATIONS

A	amperes	H	henries	N/O	normally open	RMO	rack mount only
AFC	automatic frequency control	HDW	hardware	NOM	nominal	RMS	root-mean square
AMPL	amplifier	HEX	hexagonal	NPO	negative positive zero (zero temperature coefficient)	RWV	reverse working voltage
		HG	mercury			S-B	slow-blow
BFO	beat frequency oscillator	HR	hour(s)	NPN	negative-positive-negative	SCR	screw
BE CU	beryllium copper	HZ	hertz			SE	selenium
BH	binder head			NRFR	not recommended for field replacement	SECT	section(s)
BP	bandpass	IF	intermediate freq			SEMICON	semiconductor
BRS	brass	IMPG	impregnated	NSR	not separately replaceable	SI	silicon
BWO	backward wave oscillator	INCD	incandescent			SIL	silver
		INCL	include(s)			SL	slide
CCW	counter-clockwise	INS	insulation(ed)	OBD	order by description	SPG	spring
CER	ceramic	INT	internal	OH	oval head	SPL	special
CMO	cabinet mount only			OX	oxide	SST	stainless steel
COEF	coefficient	K	kilo = 1000			SR	split ring
COM	common	LH	left hand	P	peak	STL	steel
COMP	composition	LIN	linear taper	PC	printed circuit	TA	tantalum
COMPL	complete	LK WASH	lock washer	PF	picofarads = 10^{-12} farads	TD	time delay
CONN	connector	LOG	logarithmic taper			TGL	toggle
CP	cadmium plate	LPF	low pass filter	PH BRZ	phosphor bronze	THD	thread
CRT	cathode-ray tube			PHL	Phillips	TI	titanium
CW	clockwise	M	milli = 10^{-3}	PIV	peak inverse voltage	TOL	tolerance
		MEG	meg = 10^{6}	PNP	positive-negative-positive	TRIM	trimmer
DEPC	deposited carbon	MET FLM	metal film			TWT	traveling wave tube
DR	drive	MET OX	metallic oxide	P/O	part of	U	micro = 10^{-6}
ELECT	electrolytic	MFR	manufacturer	POLY	polystyrene	VAR	variable
ENCAP	encapsulated	MHZ	mega hertz	PORC	porcelain	VDCW	dc working volts
EXT	external	MINAT	miniature	POS	position(s)		
F	farads	MOM	momentary	POT	potentiometer	W/	with
FH	flat head	MOS	metal ozide substrate	PP	peak-to-peak	W	watts
FIL H	fillister head	MTG	mounting	PT	point	WIV	working inverse voltage
FXD	fixed	MY	"mylar"	PWV	peak working voltage	WW	wirewound
G	giga (10^{9})	N	nano (10^{-9})	RECT	rectifier	W/O	without
GE	germanium	N/C	normally closed	RF	radio frequency		
GL	glass	NE	neon	RH	round head or right hand		
GRD	ground(ed)	NI PL	nickel plate				

01194-14

Table 9G-6-1. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	05307-60001	1	BOARD ASSY:LOGIC (NOT AVAILABLE FOR FIELD REPLACEMENT OR SALE)	28480	05307-60001
A1C1	0180-0210	4	C:FXD ELECT 3.3 UF 20% 15VDCW	56289	150D335X0015A2-DYS
A1C2	0180-1714	1	C:FXD ELECT 330 UF 10% 6VDCW	28480	0180-1714
A1C3	0180-0291	4	C:FXD ELECT 1.0 UF 10% 35VDCW	56289	150D105X9035A2-DYS
A1C4	0180-0291		C:FXD ELECT 1.0 UF 10% 35VDCW	56289	150D105X9035A2-DYS
A1C5	0180-0291		C:FXD ELECT 1.0 UF 10% 35VDCW	56289	150D105X9035A2-DYS
A1C6	0180-0291		C:FXD ELECT 1.0 UF 10% 35VDCW	56289	150D105X9035A2-DYS
A1C7	0150-0071	5	C:FXD CER 400 PF 5% 1000VDCW	56289	C0168102E401JS27-CDH
A1C8	0150-0071		C:FXD CER 400 PF 5% 1000VDCW	56289	C0168102E401JS27-CDH
A1C9	0150-0071		C:FXD CER 400 PF 5% 1000VDCW	56289	C0168102E401JS27-CDH
A1J1	1251-3246	3	CONNECTOR:POST TYPE 3 FEMALE CONTACT	27264	09-52-3030
A1P1	1251-2756	1	CONNECTOR:R & P, 50 CONTACT	74868	57-20500-31
A1Q1	1854-0215	2	TSTR:SI NPN	80131	2N3904
A1Q2	1853-0036	1	TSTR:SI PNP	80131	2N3906
A1Q3	1854-0215		TSTR:SI NPN	80131	2N3904
A1R1	0683-4725	10	R:FXD COMP 4700 OHM 5% 1/4W	01121	CB 4725
A1R2	0683-4725		R:FXD COMP 4700 OHM 5% 1/4W	01121	CB 4725
A1R3	0683-4725		R:FXD COMP 4700 OHM 5% 1/4W	01121	CB 4725
A1R4	0683-4715	1	R:FXD COMP 470 OHM 5% 1/4W	01121	CB 4715
A1R5	0683-4725		R:FXD COMP 4700 OHM 5% 1/4W	01121	CB 4725
A1R6	0683-2715	1	R:FXD COMP 270 OHM 5% 1/4W	01121	CB 2715
A1R7	0683-2025	7	R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1R8	0683-2025		R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1R9	0683-4725		R:FXD COMP 4700 OHM 5% 1/4W	01121	CB 4725
A1R10	0683-2025		R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1R11	0683-4725		R:FXD COMP 4700 OHM 5% 1/4W	01121	CB 4725
A1R12	0683-4725		R:FXD COMP 4700 OHM 5% 1/4W	01121	CB 4725
A1R13	0683-4725		R:FXD COMP 4700 OHM 5% 1/4W	01121	CB 4725
A1R14	0683-4725		R:FXD COMP 4700 OHM 5% 1/4W	01121	CB 4725
A1R15	0683-2025		R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1R16	0683-2025		R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1R17	0683-2025		R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1R18	0683-2025		R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1S1	3101-0551	1	SWITCH:SLIDE, MINIATURE 4P3POS	95146	MSS-4300
A1S2	3101-0552	3	SWITCH:PUSHBUTTON 2 STATION DPDT	71590	PB 15
A1U1	1820-0669	2	IC:TTL LP PRESETTABLE SYNC DEC. COUNTER	07263	U7B93L1059X
A1U2	1820-0669		IC:TTL LP PRESETTABLE SYNC DEC. COUNTER	07263	U7B93L1059X
A1U3	1820-0986	4	IC:DIGITAL	28480	1820-0986
A1U4	1820-0986		IC:DIGITAL	28480	1820-0986
A1U5	1820-0986		IC:DIGITAL	28480	1820-0986
A1U6	1820-0986		IC:DIGITAL	28480	1820-0986
A1U7	1820-0987	1	IC:TTL 1-OF-8 PRIORITY ENCODER	07263	U7B93L1859X
A1U8	1820-0710	1	IC:DIGITAL TTL+LOGIC 5V 5%	07263	U7B93L2259X
A1U9	1820-0658	4	IC:TTL LOW POWER 8-INPUT MULTIPLEXER	07263	U7B93L1258X
A1U10	1820-0658		IC:TTL LOW POWER 8-INPUT MULTIPLEXER	07263	U7B93L1259X
A1U11	1820-0658		IC:TTL LOW POWER 8-INPUT MULTIPLEXER	07263	U7B93L1259X
A1U12	1820-0658		IC:TTL LOW POWER 8-INPUT MULTIPLEXER	07263	U7B93L1259X
A1U13	1820-0782	1	IC:TTL TRIPLE 3-INPT NOR GATE	01295	SN7427N
A1U14	1820-0617	1	IC:TTL QUAD 2-INPT EXCL. NOR GATE	04713	MC3022P
A1U15	1820-0628	1	IC:DIGITAL TTL 64-BIT R/W MEMORY	01295	SN7489N
A1U16	1820-0084	1	IC:TTL 4W 2-INPT AND/OR GATE	01295	SN7453N
A1U17	1820-0586	1	IC:TTL LP HEX INVERTER	12040	DM74L04N
A1U18	1820-0304	1	IC:TTL J-K M/S F/F W/CLOCKED & INPTS	01295	SN7472N
A1U19	1820-0072	1	IC:TTL DUAL 2W 2-INPT AND/OR GATE	01295	SN7450N
A1U20	1820-0328	1	IC:TTL QUAD 2-INPT NOR GATE	04713	SN7402N
A1U21	1820-0056	1	IC:TTL DIVIDE BY 12 10 MHZ MIN.	01295	SN7492N
A1U22	1820-0068	1	IC:TTL TRIPLE 3-INPUT POS NAND GATE	12040	SN7410N
A1U23	1820-1085	1	IC:DIGITAL TTL	07263	U7B9L2459X
A1U24	1820-0587	1	IC:TTL LP TRIPLE 3-INPT NAND GATE	12040	DM74L10N
A1U25	1820-0382	1	IC:TTL HS 2 W 4-INPT AND OR INV GATE	01295	SN74H55N
A1U26	1820-0661	1	IC:TTL QUAD 2-INPT OR GATE	01295	SN7432N
A1U27	1820-0281	2	IC:DIGITAL DUAL J-K MASTER SLAVE F/F	04713	SN74107N
A1U28	1820-0281		IC:DIGITAL DUAL J-K MASTER SLAVE F/F	04713	SN74107N
A1U29	1820-0054	1	IC:TTL QUAD 2-INPT NAND GATE	01295	SN7400N
A1U30	1820-0777	1	IC:TTL LOW POWER BCD TO DECODER	01295	SN74L42N
A1U31	1820-0701	1	IC:TTL LOW POWER QUAD LATCH	07263	U7B93L1459X
A1U32	1820-0600	1	IC:TTL LP DECADE COUNTER	12040	DM85L90N

See introduction to this section for ordering information

Table 9G-6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2	05307-60002	1	BOARD ASSY:INPUT	28480	05307-60002
A2C1	0170-0038	1	C:FXD MY 0.22 UF 10% 200VDCW	56289	148P22492 PUM
A2C2	0160-2250	1	C:FXD CER 5.1 PF 500VDCW	72982	301-000-C0H0-519E
A2C3	0160-0362	1	C:FXD MICA 510PF 5%	28480	0160-0362
A2C4	0150-0071		C:FXD CER 400 PF 5% 1000VDCW	56289	C0168102E401JS27-C0H
A2C5	0140-0217	2	C:FXD MICA 140 PF 2%	28480	0140-0217
A2C6	0160-3060	2	C:FXD CER 0.1 UF 20% 25VDCW	56289	3C42A-CML
A2C7	0160-0194	1	C:FXD MY 0.015 UF 10%	56289	192P15392-PTS
A2C8	0160-3060		C:FXD CER 0.1 UF 20% 25VDCW	56289	3C42A-CML
A2C9	0180-0210		C:FXD ELECT 3.3 UF 20% 15VDCW	56289	150D335X0015A2-DYS
A2C10	0180-0210		C:FXD ELECT 3.3 UF 20% 15VDCW	56289	150D335X0015A2-DYS
A2C11	0180-1701	1	C:FXD ELECT 6.8 UF 20% 6VDCW	28480	0180-1701
A2C12	0150-0071		C:FXD CER 400 PF 5% 1000VDCW	56289	C0168102E401JS27-C0H
A2C13	0180-0155	1	C:FXD ELECT 2.2 UF 20% 20VDCW	56289	150D225X0020A2-DYS
A2C14	0180-0106	1	C:FXD ELECT 60 UF 20% 6VDCW	28480	0180-0106
A2C15	0150-0075	2	C:FXD CER 4700 PF +100-20% 500VDCW	72982	851-000-X500-472Z
A2C16	0150-0075		C:FXD CER 4700 PF +100-20% 500VDCW	72982	851-000-X500-472Z
A2C17	0180-0373	1	C:FXD ELECT 0.68 UF 10% 35VDCW	56289	150D684X9035A2-DYS
A2C18	0160-0134	1	C:FXD MICA 220PF 5% 300VDCW	14655	RDM15F121J3C
A2C19	0180-0210		C:FXD ELECT 3.3 UF 20% 15VDCW	56289	150D335X0015A2-DYS
A2CR1	1901-0040	2	DIODE:SILICON 50 MA 30 WV	07263	FDG1088
A2CR2	1901-0579	2	DIODE:SI(SPECIAL)	03508	SE 445
A2CR3	1901-0040		DIODE:SILICON 50 MA 30 WV	07263	FDG1088
A2CR4	1901-0579		DIODE:SI(SPECIAL)	03508	SE 445
A2CR5	1902-3193	2	DIODE BREAKDOWN:13.3V 5%	28480	1902-3193
A2CR6	1902-3193		DIODE BREAKDOWN:13.3V 5%	28480	1902-3193
A2CR7	1902-3048	2	DIODE BREAKDOWN:SILICON 3.48V 5%	28480	1902-3048
A2CR8	1902-3048		DIODE BREAKDOWN:SILICON 3.48V 5%	28480	1902-3048
A2CR9	1902-3182	1	DIODE BREAKDOWN:SILICON 12.1V 5%	28480	1902-3182
A2P1	1251-3247	3	CONNECTOR:PIN-WAFER ASSY	28480	1251-3247
A2P2	1251-0584	1	CONNECTOR:POST TYPE, NYLON 9-PINS	27264	09-59-1092(A-2373-9A
A2Q1	1855-0308	1	TSTR:SI NPN DUAL	28480	1855-0308
A2R1	0757-0344	1	R:FXD MET FLM 1.00 MEGOHM 1% 1/4W	28480	0757-0344
A2R2	0757-0442	3	R:FXD MET FLM 10.0K OHM 1% 1/8W	28480	0757-0442
A2R3	0683-2215	1	R:FXD COMP 220 OHM 5% 1/4W	01121	CB 2215
A2R4	0686-1045	1	R:FXD COMP 100K OHM 5% 1/2W	01121	EB 1045
A2R5	0757-0442		R:FXD MET FLM 10.0K OHM 1% 1/8W	28480	0757-0442
A2R6	0757-0442		R:FXD MET FLM 10.0K OHM 1% 1/8W	28480	0757-0442
A2R7	2100-1984	1	R:VAR FLM 100 OHM 10% LIN 1/2W	28480	2100-1984
A2R8	0698-3161	1	R:FXD MET FLM 38.3K OHM 1% 1/8W	28480	0698-3161
A2R9	0683-7515	1	R:FXD COMP 750 OHM 5% 1/4W	01121	CB 7515
A2R10	0683-1055	1	R:FXD COMP 1 MEGOHM 5% 1/4W	01121	CB 1055
A2R11	0683-8215	1	R:FXD COMP 820 OHM 5% 1/4W	01121	CB 8215
A2R12	0683-3315	2	R:FXD COMP 330 OHM 5% 1/4W	01121	CB 3315
A2R13	0683-5115	1	R:FXD COMP 510 OHM 5% 1/4W	01121	CB 5115
A2R14	0683-3315		R:FXD COMP 330 OHM 5% 1/4W	01121	CB 3315
A2R15	0683-0825	2	R:FXD COMP 8.2 OHM 5% 1/4W	01121	CB 82G5
A2R16	0683-1015	3	R:FXD COMP 100 OHM 5% 1/4W	01121	CB 1015
A2R17	0683-2035	2	R:FXD COMP 20K OHM 5% 1/4W	01121	CB 2035
A2R18	0683-2035		R:FXD COMP 20K OHM 5% 1/4W	01121	CB 2035
A2R19	0683-3025	4	R:FXD COMP 3000 OHM 5% 1/4W	01121	CB 3025
A2R20	0683-3025		R:FXD COMP 3000 OHM 5% 1/4W	01121	CB 3025
A2R21	0683-3025		R:FXD COMP 3000 OHM 5% 1/4W	01121	CB 3025
A2R22	0683-1015		R:FXD COMP 100 OHM 5% 1/4W	01121	CB 1015
A2R23	0683-0825		R:FXD COMP 8.2 OHM 5% 1/4W	01121	CB 82G5
A2R24	0683-3025		R:FXD COMP 3000 OHM 5% 1/4W	01121	CB 3025
A2R25	0683-4725		R:FXD COMP 4700 OHM 5% 1/4W	01121	CB 4725
A2R26	2100-2517	1	R:VAR FLM 50K OHM 10% LIN 1/2W	28480	2100-2517
A2R27	0683-1015		R:FXD COMP 100 OHM 5% 1/4W	01121	CB 1015
A2S1	3101-0552		SWITCH:PUSHBUTTON 2 STATION DPDT	71590	PB 15
A2S2	3101-0552		SWITCH:PUSHBUTTON 2 STATION DPDT	71590	PB 15
A2U1	1826-0065	1	IC:LINEAR, VOLTAGE COMPARATOR	12040	LM311N
A2U2	1826-0055	1	IC:LINEAR DUAL COMPARATOR	07263	U6A7711393
A2U3	1820-0875	1	IC:DIGITAL TTL MONOSTABLE MULTIVIBRATOR	07263	U6A960059X

Table 9G-6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			MISCELLANEOUS & CHASSIS MOUNTED PARTS		
	0340-0733	2	INSULATOR:BINDING POST BLACK	28480	0340-0733
	0340-0734	2	INSULATOR:BINDING POST RED	28480	0340-0734
	0360-0124	9	TERMINAL:SOLDER LUG	28480	0360-0124
	0370-0914	6	BEZEL:PUSHBUTTON KNOB JADE GREY	28480	0370-0914
	0370-0970 OR	6	PUSHBUTTON (BLACK AND GRAY)	28480	0370-0970
	0370-2486	6	PUSHBUTTON (SOLID GRAY)	28480	0370-2486
	0370-1005	1	KNOB:JADE GREY	28480	0370-1005
	0380-0310	3	STANDOFF	00000	OBD
	0380-0311	3	SPACER:THREADED CAPTIVE 1/2 LG	28480	0380-0310
	0905-0479	1	GASKET	28480	0905-0479
	1200-0475	7	SOCKET:IC SINGLE LEAD	70998	75060-00
	1460-1311	1	SPRING: LEAF	28480	1460-1311
	1460-1312	1	SPRING: LEAF	28480	1460-1312
J1	1510-0084	1	BINDING POST	28480	1510-0084
J2	1510-0087	1	BINDING POST:BLACK	28480	1510-0087
R1	2100-0566	1	R:VAR COMP 5K OHM 20% 10 CCW 1/2W	28480	2100-0566
	3050-0279	2	WASHER:FIBER 7/16" OD 1/4" ID	82389	S-1564
	5040-7032	1	FOOT	28480	5040-7032
	05300-20010	1	CASE	28480	05300-20010
	05300-40003	4	SUPPORT:BOARD	28480	05300-40003
	05300-40004	4	GUIDE:SLIDE	28480	05300-40004
	05300-80004	1	LABEL:POWER LINE	28480	05300-80004
	05301-00004	1	PANEL:REAR	28480	05301-00004
	05301-20005	1	STAND:TILT	28480	05301-20005
	05301-40001	1	FOOT	28480	05301-40001
	05307-00001	1	PANEL:FRONT	28480	05307-00001
	05307-00002	2	BRACKET	28480	05307-00002
	05307-00003	1	SHIELD:LOGIC	28480	05307-00003
	05307-00004	1	SHIELD:INPUT	28480	05307-00004

See introduction to this section for ordering information

Table 9G-6-2. Manufacturers Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	U.S.A. COMMON	ANY SUPPLIER OF U.S.A.	
01121	ALLEN BRADLEY CO.	MILWAUKEE, WIS.	53204
01295	TEXAS INSTRUMENTS INC. SEMICONDUCTOR COMPONENTS DIV.	DALLAS, TEX.	75231
03508	G.E. CO. SEMICONDUCTOR PROD. DEPT.	SYRACUSE, N.Y.	13201
04713	MOTOROLA SEMICONDUCTOR PROD.INC.	PHOENIX, ARIZ.	85008
07263	FAIRCHILD CAMERA & INST. CORP. SEMICONDUCTOR DIV.	MOUNTAIN VIEW, CALIF.	94040
12040	NATIONAL SEMICONDUCTOR CORP.	DANBURY, CONN.	06810
14655	CORNELL DUBLIER ELECT. DIV.FEDERAL PACIFIC ELECT. CO.	NEWARK, N.J.	07105
27264	MOLEX PROD. CO.	DOWNERS GROVE, ILL.	60515
28480	HEWLETT-PACKARD CO. CORPORATE HQ	YOUR NEAREST HP OFFICE	
56289	SPRAGUE ELECTRIC CO.	N. ADAMS, MASS.	01247
70998	BIRD ELECTRONICS CORP.	CLEVELAND, OHIO	44139
71590	GLOBE UNION INC. CENTRALAB DIV.	MILWAUKEE, WISC.	53201
72982	ERIE TECHNOLOGICAL PROD. INC.	ERIE, PA.	16512
74868	AMPHENOL CORP. RF DIV.	DANBURY, CONN	06810
80131	ELECTRONIC INDUSTRIES ASSOCIATION	WASHINGTON D.C.	20006
82389	SWITCHCRAFT INC.	CHICAGO, ILL.	60630
95146	ALCO ELECT. PROD. INC.	LAWRENCE, MASS.	01843

SECTION IX G
5307A HIGH RESOLUTION COUNTER

SUBSECTION VII
MANUAL CHANGES AND OPTIONS

9G-7-1. INTRODUCTION

9G-7-2. This subsection provides the information necessary to update this manual to cover newer instruments and to backdate the manual to cover older instruments. Additionally, any available instrument options are documented in this subsection.

9G-7-3. MANUAL CHANGES

9G-7-4. Section IX G applies directly to counters having a serial number prefix of 1308. For information about instruments with different serial number prefixes, refer to the following paragraphs.

9G-7-5. Newer Instruments

9G-7-6. Newer instruments may have higher serial number prefixes than those listed on the title page of this document. The manuals for these instruments will be supplied with "manual changes" sheets that describe all changes to the manual or with replacement pages for those pages in the manual that require modification. If the updating information is missing, contact the local HP Sales and Service Office for information.

9G-7-7. Older Instruments

9G-7-8. No older instruments than those covered by this document have been manufactured.

9G-7-9. OPTIONS

9G-7-10. No options were available for the counter at the time this document was printed.

SECTION IX G
5307A HIGH RESOLUTION COUNTER

SUBSECTION VIII
CIRCUIT DIAGRAMS

9G-8-1. INTRODUCTION

9G-8-2. This subsection of the manual contains the following information:

a. A signal list that gives the signal name and connector pin number of each signal line that interconnects with the mainframe (see Table 9G-8-1).

b. A block diagram of the counter (see Figure 9G-8-1).

c. Component location views of the printed-circuit boards (part of Figure 9G-8-2).

d. A schematic diagram of the counter (part of Figure 9G-8-2).

Table 9G-8-1. Signal Interconnection List

PIN NO.	SIGNAL NAME	DESCRIPTION
1	+5 V	
2	-5 V	
3	-17 V	
4←→49	GROUND	
5*	F1	This is the signal to be accumulated in the mainframe counter.
6	$\overline{\text{"9"}}$	No Connection.
7*	F2	The input signal to the mainframe time base gated by the control circuit.
8	$\overline{\text{INHIBIT}}$	High during the measurement cycle, low during the display cycle.
9*	$\overline{\text{OPEN}}$	Low signal forces the main gate flip-flop in the mainframe to the open position.
10	$\overline{\text{CLOSE}}$	No Connection
11	$\overline{\text{LOG}}$	No Connection.
12	$\overline{\text{MGFF}}$	No Connection.
13	$\overline{\text{EXPONENT}}$	Inverted log pulses while main gate in mainframe is open, indicate number of auto ranging steps.
14	NOT USED	No Connection.
15	RESET	High signal resets all circuits.

Table 9G-8-1. Signal Interconnection List (Continued)

PIN NO.	SIGNAL NAME	DESCRIPTION
16	CLOCK	10 MHz reference signal from crystal oscillator.
17*	$\overline{\text{MAX TIME}}$	Low signal enables closing of the gate in mainframe on next log pulse. Rising edge initiates display cycle.
18	TIME BASE OUTPUT	Output from the mainframe's time base decade that is selected by the time base select code on pins 22, 23 and 24.
19	$\overline{\text{PRINT}}$	Low signal provides print command to rear panel connector of mainframe.
20	$\overline{\text{TRANSFER}}$	Low signal transfers data to display. High signal stores data.
21*	1 MHz TIME BASE INPUT	Input direct from plug-on bypasses control circuit.
22*	TIME BASE SELECT A	Time base select code (A,B, and C) determines the frequency of the time base output at pin 18.
23*	TIME BASE SELECT B	
24*	TIME BASE SELECT C	
25—50	+20 V	Full wave rectified voltage from the power transformer in the mainframe. Pin 25 is connected via the plug-on to pin 50.
26	+17 V	
27*	$\overline{\text{Hz}}$	Pins 27 and 28 provide the drive to the annunciator lights on the front panel of the mainframe. A low signal lights the corresponding indicator.
28*	$\overline{\text{M}}$	
29	$\overline{\text{S}}$	No Connection.
30	$\overline{\text{K}}$	No Connection.
31	$\overline{\mu}$	No Connection.
32*	$\overline{\text{MANUAL RESET}}$	Low signal from front-panel pushbutton switch or rear panel input clears the system to zero.
33*	$\overline{\text{DP1}}$	Low signal activates decimal point 1.
34*	$\overline{\text{DP2}}$	Low signal activates decimal point 2.
35	RIGHT/LEFT	Code indicating half character which is being addressed. High when right-hand half of character is displayed.

Table 9G-8-1. Signal Interconnection List (Continued)

PIN NO.	SIGNAL NAME	DESCRIPTION
36	DIGIT ADDRESS X	Digit address code X, Y, Z from the display scanner indicates a digit being displayed.
37	DIGIT SELECT X	Digit select code X, Y, Z is the corresponding code which selects the digit at the output of the counter. If the mainframe counter is displayed directly the corresponding lines of the digit address code and the the digit select code are connected together.
38	DIGIT ADDRESS Y	
39	DIGIT SELECT Y	
40	DIGIT ADDRESS Z	
41	DIGIT SELECT Z	
42	DATA "B"	No Connection
43	DATA "C"	No Connection.
44	DATA "D"	No Connection.
45	DATA "A"	No Connection.
46*	$\overline{DP3}$	Low signal activates decimal point 3.
47*	$\overline{DP4}$	Low signal activates decimal point 4.
48*	$\overline{DP5}$	Low signal activates decimal point 5.
49 ⟶ 4	GROUND	
50 ⟶ 25	DC IN	DC power to mainframe power supply from pin 25.

*Indicates that signal source is within counter plug-on.

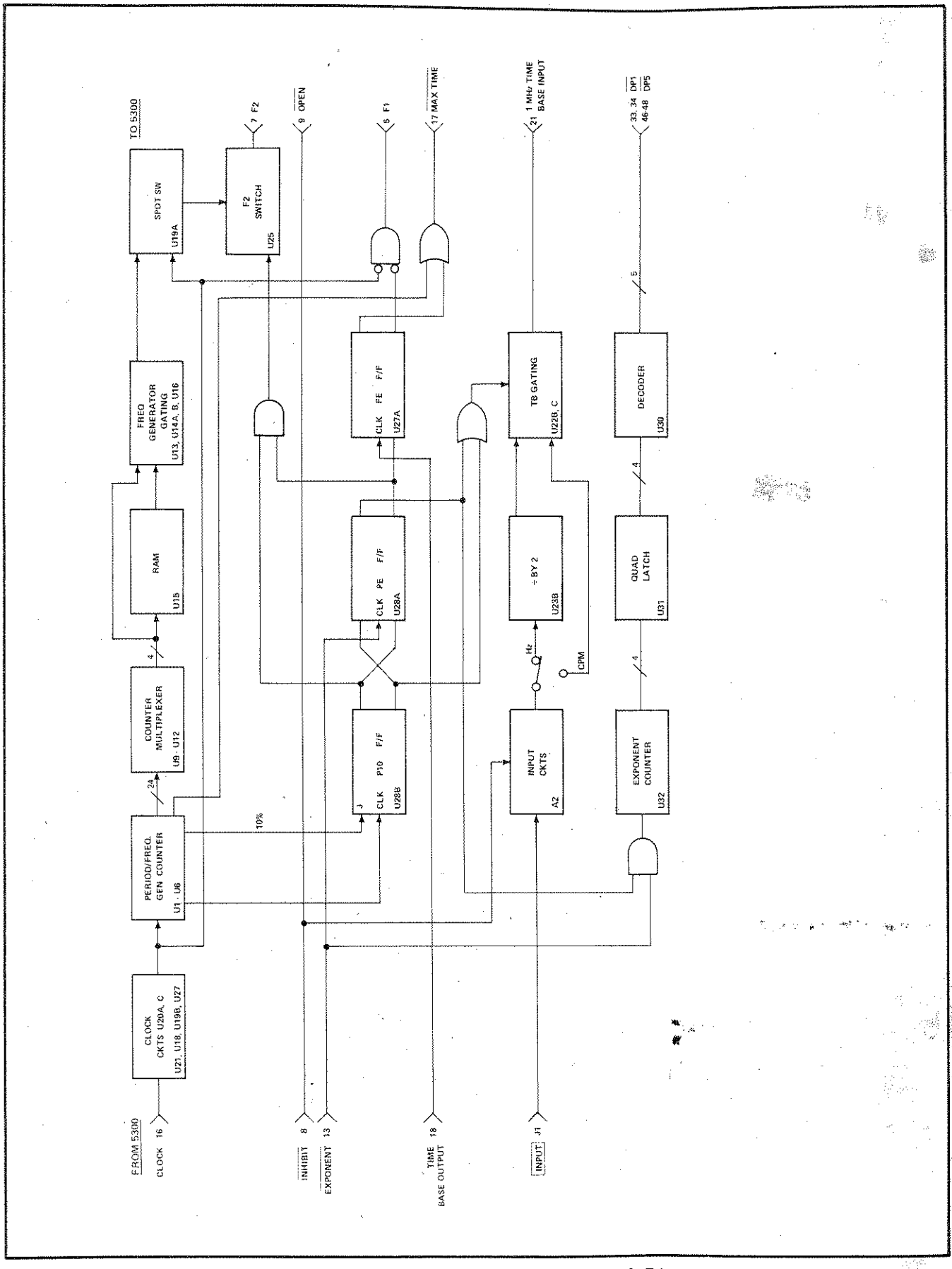
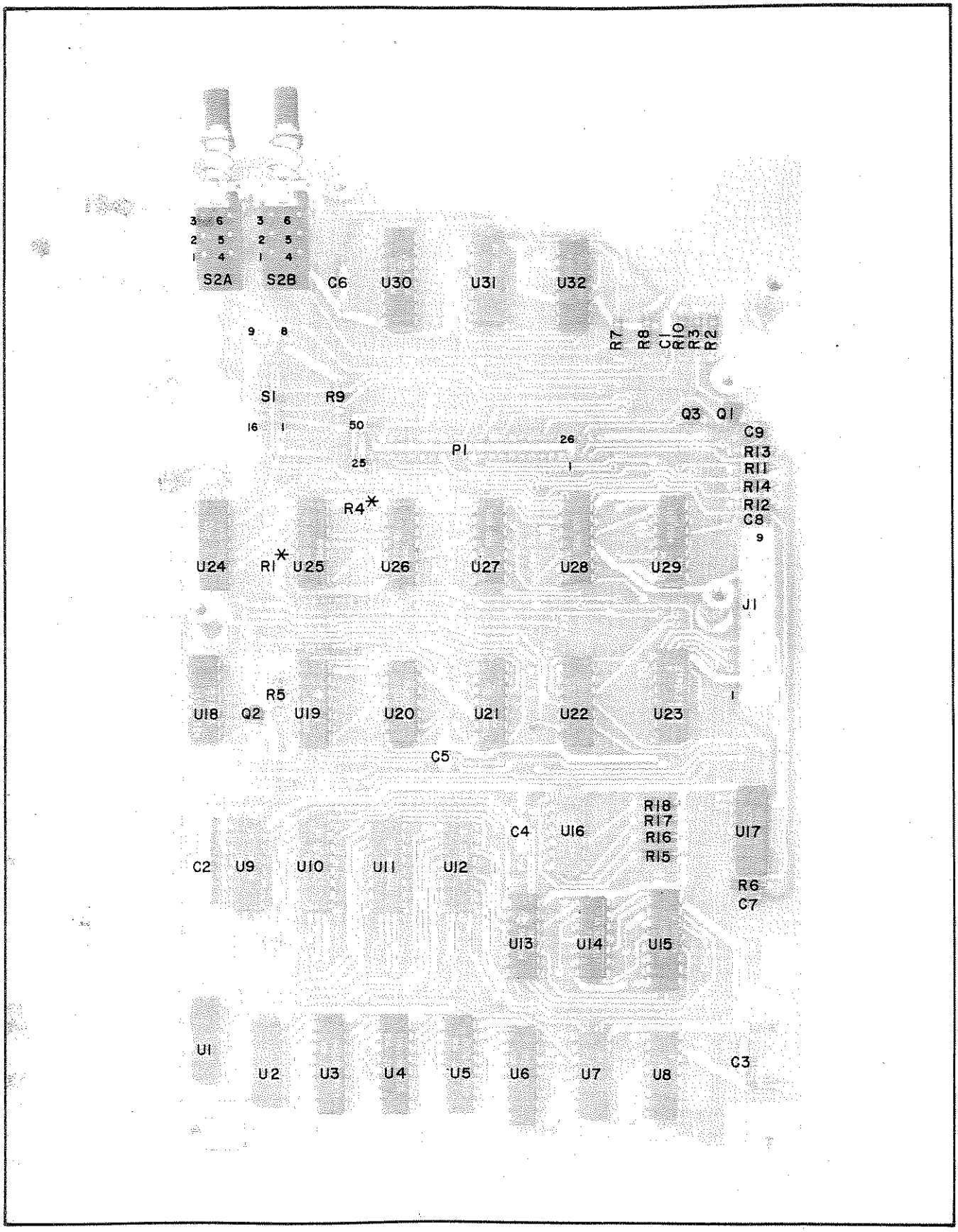


Figure 9G-8-1. 5307A Simplified Block Diagram


S2A
S2B
C6
U30
U31
U32
R7
R8
C1
R10
R3
R2
S1
R9
Q3
Q1
C9
R13
R11
R14
R12
C8
P1
R4*
R1*
U24
U25
U26
U27
U28
U29
J1
R5
U18
Q2
U19
U20
U21
U22
U23
C5
R18
R17
R16
R15
C4
U16
U17
C2
U9
U10
U11
U12
R6
C7
U13
U14
U15
U1
U2
U3
U4
U5
U6
U7
U8
C3

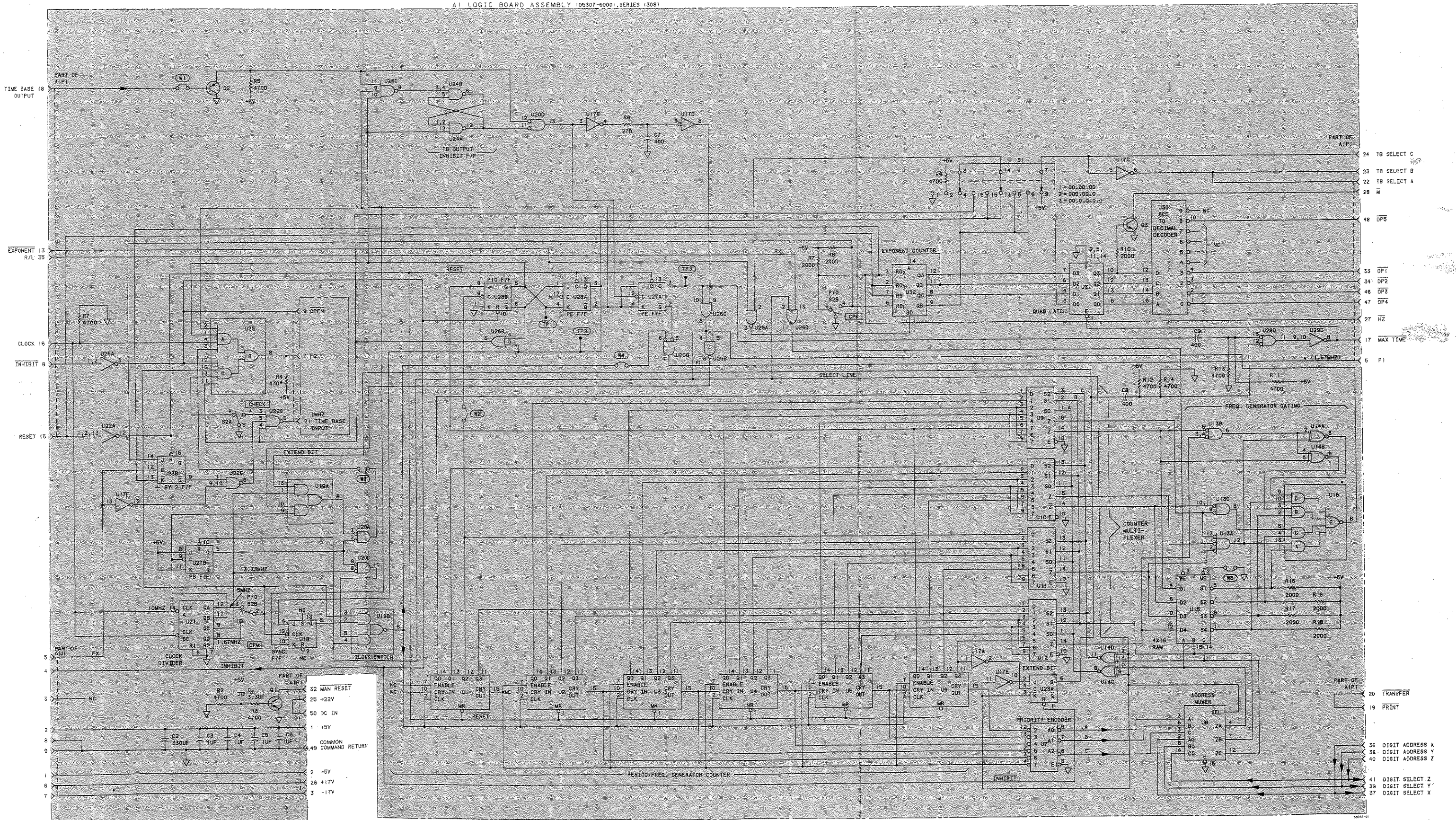
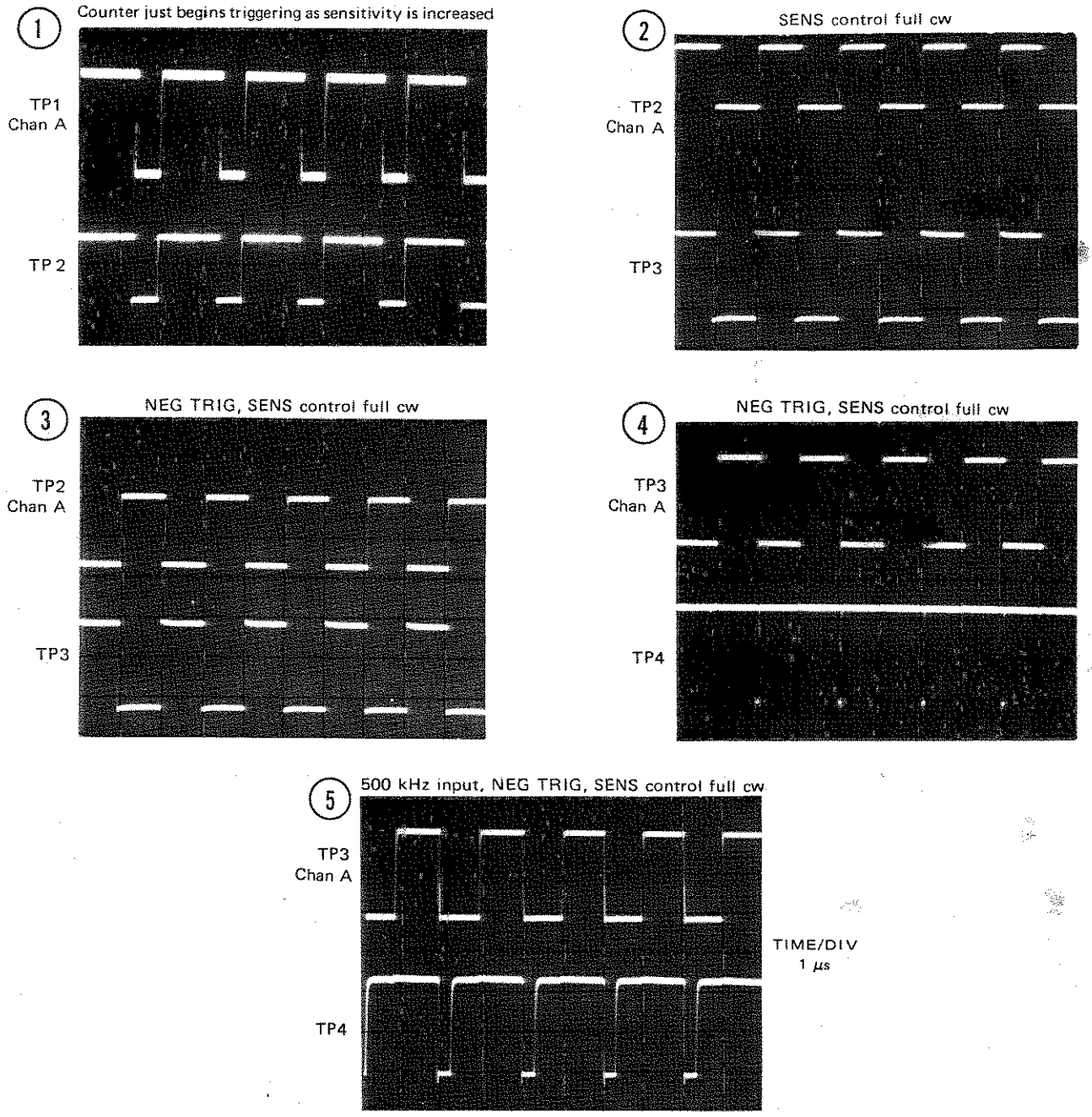


Figure 9G-8-2. A1 Logic Board Assembly

Part of Figure 9G-8-3. A2 Input Board Assembly (A2 Waveforms)

A2 Waveforms



Oscilloscope Setting (unless otherwise indicated):

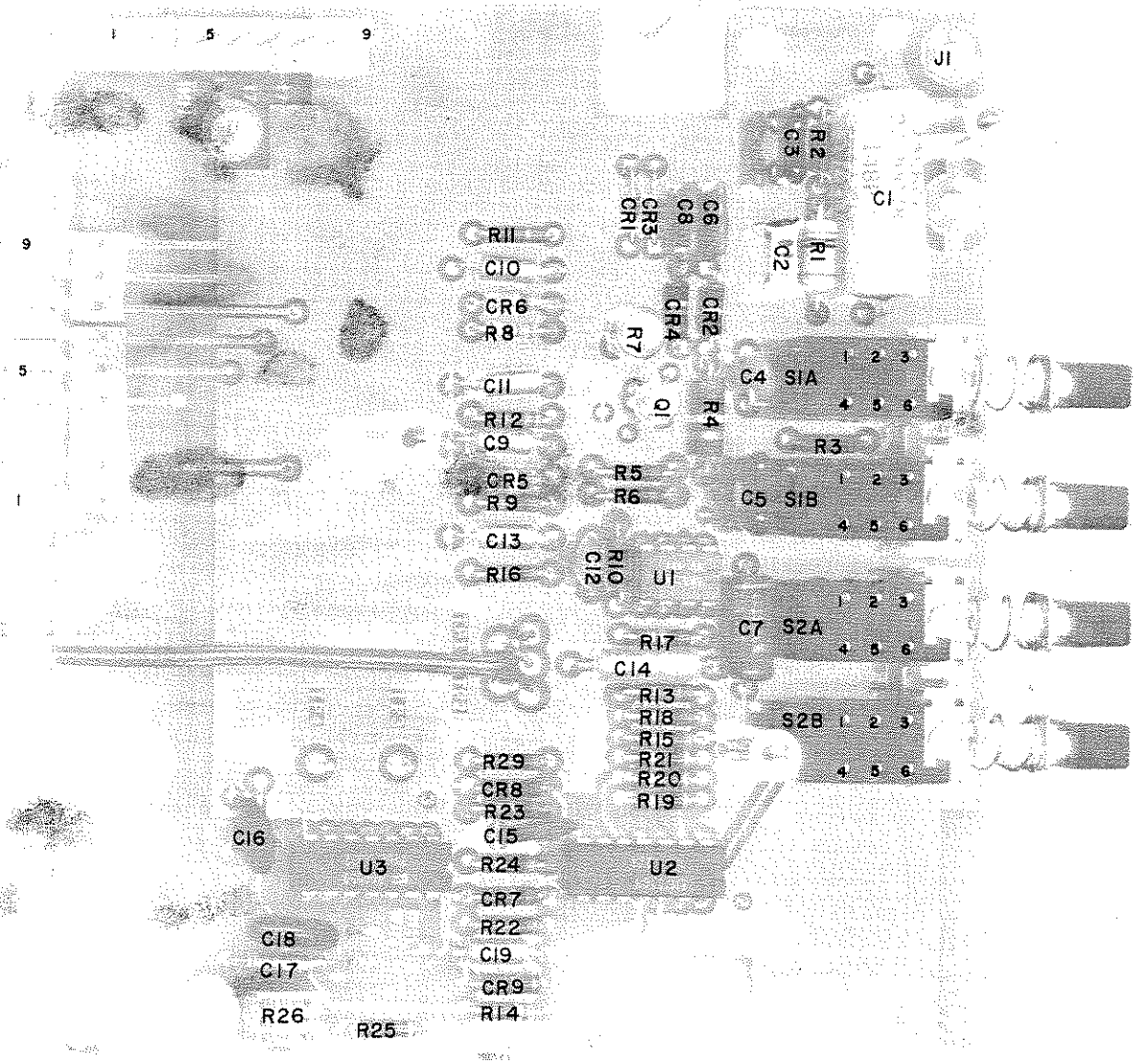
POLARITY (both channels)	+up
Coupling (both channels)	DC
DISPLAY	ALT
TIME/CM	10 μs
VOLTS/CM (Chan A)	.05
VOLTS/CM (Chan B)	.2
TRIGGER	INT
SLOPE	+

Use 10:1 divider probes

Counter:

POS TRIG

Input Signal	50 kHz	3V p-p
SENSITIVITY control		full ccw


J1
C1
C2
C3
R1
R2
C4 S1A
C5 S1B
R3
C7 S2A
S2B
C6
C8
CR1
CR3
R11
C10
CR6
R8
C11
R12
C9
CR5
R9
C13
R16
R7
CR4
CR2
Q1
R4
R5
R6
C12
R10
U1
R17
C14
R13
R18
R15
R21
R20
R19
R29
CR8
R23
C15
R24
U2
CR7
R22
C19
CR9
R14
C16
U3
C18
C17
R26
R25

A2 INPUT BOARD ASSEMBLY (05307-60002, SERIES 1308)

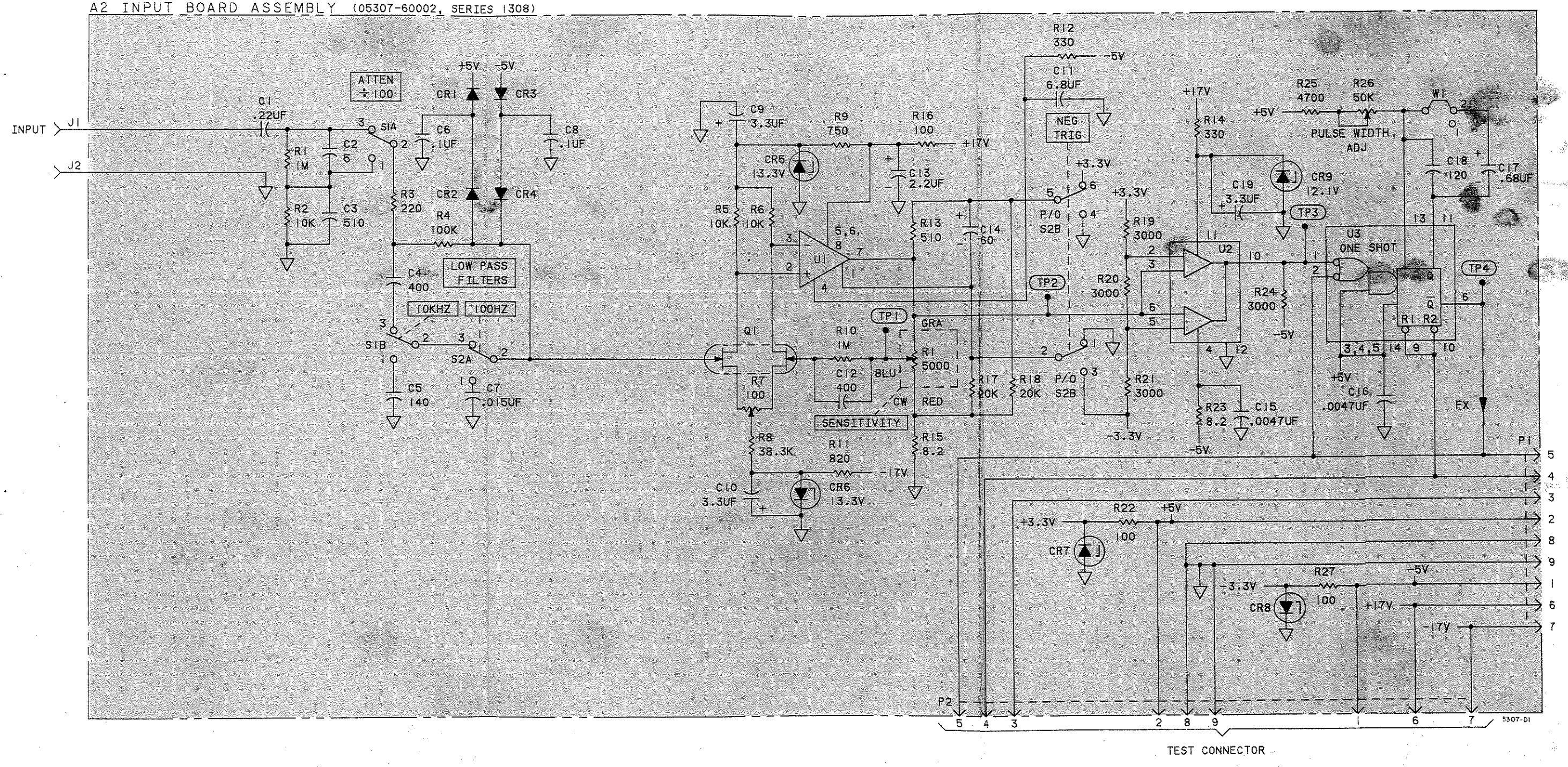


Figure 9G-8-3. A2 Input Board Assembly